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Design and Implementation of Reversible RAM

Mrs. G. SRILAKSHMI[1], MATTA SUDHA ANANTHA SRI[2], MOHAMMED SADIYARIZA[3], RANDHI VEDA SAI[4], RAYAPROLU V S S L N DHATHRI[5], KOTA DURGA PRASAD[6]

[1]Assistant Professor, Dept. of ECE, PRAGATI ENGINEERING COLLEGE

[23456]UG Students, Dept. of ECE, PRAGATI ENGINEERING COLLEGE

ABSTRACT

In the modern digital-world, power dissipation in microprocessors is becoming a significant challenge for the researchers to design an efficient reversible logic circuit. Reversible logic has become immensely popular research area and its applications have spread in various technologies for their low power consumption. In this paper we proposed an efficient design of random access memory using reversible logic. In the way of designing the reversible random access memory we proposed a reversible decoder and a write enable reversible master slave D flip-flop. All the reversible designs are superior in terms of quantum cost, delay and garbage outputs compared to the designs existing in literature.

INTRODUCTION

Ternary content Addressable memory is a one of the Special type of memory ,these memory has the three logic states ie: Logic “0”, Logic “1” and Logic” x” this is used to perform the search operation within the Single Clock Cycle. TCAM finds the application in various fields. The main application of TCAM is found in the Network Routers where searching operation is done using the Contents. The other applications of the TCAM are found in Intrusion Detect, image processing, Gene pattern searching bioinformatics. The proposed concept is designed using the reversible logic gate. In Reversible logic gates, each and every computed information is stored, because of that there is no loss of data and loss of power. There are equal number of inputs and outputs in reversible gates and the information is reused in the circuit by avoiding the loss of information by not computing the information computed before. There are three factors in the reversible logic, Quantum cost, worst case Delay and Garbage outputs. There are few gates proposed namely Toffoli Gate which has the quantum cost of 5 which has 3 inputs and 3 outputs and Feyman gate has quantum cost of 1 and has two inputs and two outputs similarly many reversible gates have been proposed satisfying all the reversible properties. RAM needs an address to fetch the data stored in the memory whereas CAM needs the contents to be searched in the search lines and the matched address is obtained at the output. CAM is known for its high speed search operation. However, the CAMs consume lot of power due to its high speed operation and lot of heat is dissipated. High power consumption in CAM devices increases the junction temperatures of the chip which increases the heat dissipation there by reducing the performance of the chip [1]. When there is computation in any logic circuits, the loss in information will lead to heat generation in the system. Landauer [2] proposed that for every single

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bit loss of information there will be KTln2 Joules of energy will be dissipated in the form of heat. Bennett [3] showed that heat dissipation will be zero ideally if the circuit is designed using reversible elements. According to the definition of reversible elements, the circuit is said to be reversible if there is no loss in information. Feynman [4] has proposed the first 2×2 reversible gate which will do ex or operation. Now-a-days, the research in designing the irreversible circuits to reversible circuits is the great area of concern due to its low power characteristics of the design. In the conventional TCAM design, 16 transistors are used to do the search and match operations. The change in state of the transistors due to the changes in the bit of search line and matchline will lead to the heat dissipation of the circuits. It has been shown that the power consumption for the conventional 16T TCAM cell is approximately 12mW to 15mW of power [5]. This paper aims at presenting a novel TCAM design using reversible elements as an alternate to reduce the power consumption in the TCAM cell. A novel SRAM cell is designed using the reversible elements which are used to store the data. The match line and the search line are also designed using reversible elements which emulate the conventional NAND type TCAM cell. To the best of our knowledge, this is the first paper on designing a novel TCAM cell using reversible elements. The design is verified by using Xilinx ISE simulator.

LITERATURE SURVEY

More research is done on the reversible logic gates. The processing of the reversible logic gates is a basic method of reusing [1].Using the TR gate a binary subtractor is proposed , TR gates stands better than that of the other reversible gates available and by using this reversible logic gate the garbage output ,quantum cost and circuit complexity is reduced .TCAM is used in many High speed searching applications one of the well-known application is Internet Router, where CAM or TCAM is used to search the content of the memory and gives out the Address of respective memory to the RAM[2].There are many applications of reversible logic gates in Low Power CMOS which are used in CODE Converters, Bioinformatics which are designed by utilizing the Basic available Reversible logic gates . Converters reduce the switching activities by pointing the transition between single and many ordered logical operations [3]. Cam Compares the stored bits with the search line bit which is fed from the input side and there are two types of CAM ie Binary CAM and Ternary CAM. Binary CAM has only Two states “logic 0” and logic”1” and in Ternary CAM there are Three states Logic “1” ,Logic “0” and Don’t Care , Hashing technique is used in CAM Based RAMS which is nothing but the conversion of long data into the short Key .

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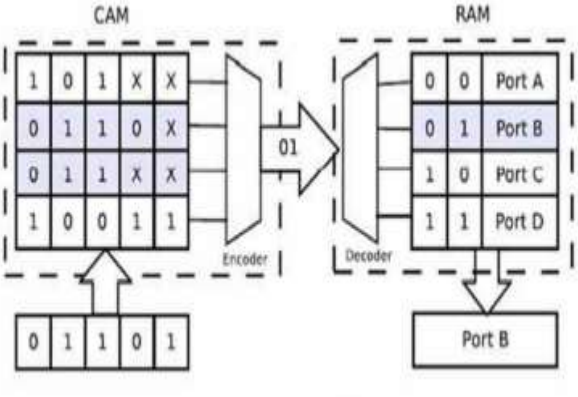
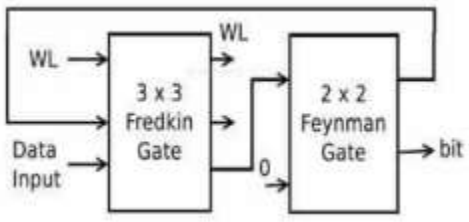
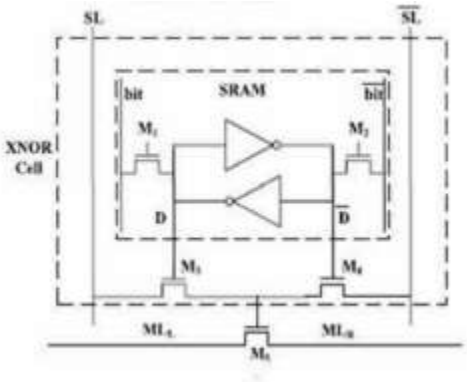


BASIC REVERSIBLE LOGIC GATES AND OPERATION

Reversible Logic gates are nothing but the gates having the same number of inputs as well as same number of outputs. Where the inputs and outputs of the gate are mapped with each other. There are 3 factors related to the reversible logic gates, Quantum cost, Worst case delay and garbage outputs. Feyman gate which is said to be controlled Not gate having two inputs and two outputs which is said to be 2x2 and having the quantum cost of 1with worst case delay of 1. Fredkin gate is 3x3 reversible gate having the quantum cost of 5 and worst case delay of 5. Tofoli gate is 3x3 one of the reversible gate having the quantum cost of 6 with worst case delay of 6.peres gate is also 3x3 the member of reversible logic gate family with quantum cost of 4 with worst case delay of 4.





Working of SRAM and TCAM and Reversible TCAM:

In this section we are going to discuss about the SRAM using reversible logic gates and about the conventional TCAM realized using the Conventional logic gates. Figure 6 shows the realization of the SRAM using reversible logic gates. Here in proposed design we use 3x3 Fredkin gate and 2x2 Feyman gate to realize the SRAM. This SRAM has the capacity to store single bit of data in it. SRAM has two states Hold state and Read/Write State. The operating modes of the SRAM Depends upon the WL when WL=0 SRAM operates in Hold State and When WL=1 SRAM operates in Read/ Write Mode. Figure 7 shows the Diagram of Conventional TCAM. it consists of Two back inverted inverters connected to each other in opposite direction which acts as a memory to store a data it consists of SL and SL_bar which are known as search lines which are used to search the bit stored in the memory and ML(match line) which is output of the TCAM. In this part we discuss about the Single bit TCAM Realized Using the Reversible Logic gates. The Input data is given from the SRAM to the TCAM cell as a input to Feyman gate which is then

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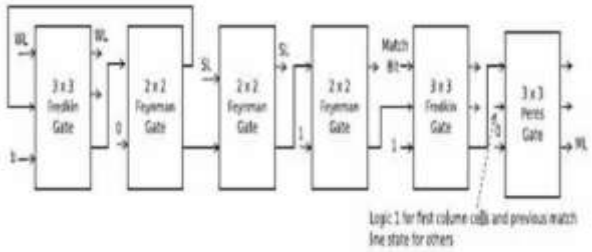
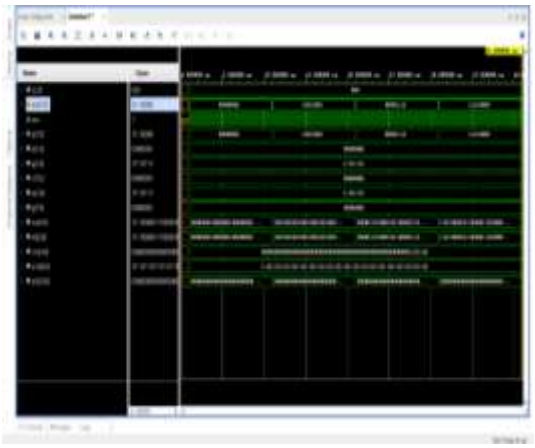
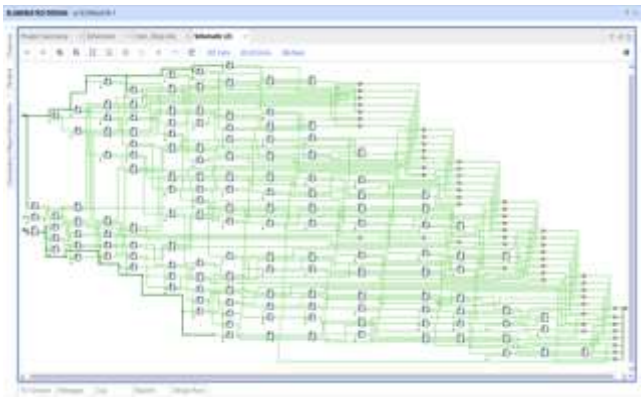
connected to Feyman gate and then connected to the Fredkin gate the exored results is given as input to the to peres gate where output is obtained at Match line(ML) the same TCAM can be Realized by replacing the Peres gate by Tofoli gate .But the quantum cost of the Second design increases slightly which also effects the worst case delay of the circuit also but garbage outputs remain same for the both the design.





Above two Designs perform the same operations which are verified on Xilinx ISE 14.7 simulator and compared the designs in terms of cost performance and garbage Outputs which varies slightly In above designs we have only tried to reduce the quantum cost and delay of the circuit and compare the both the design for single bit we can also design for array of cells and compare the results which is also done using Xilinx tool and verified on FPGA kit. This paper proposed a novel design of TCAM design using reversible circuit design. Ternary content addressable memory compares input data against stored data (logic '0', logic '1', don't care) in parallel and outputs the matched data. In reversible SRAM design, 3 × 3 Fredkin gate and the 2 × 2 Feynman gate is used to form the SRAM cell which is used to store the single bit of information. Each and every SRAM cell will have word line (WL) in order to make the SRAM cell to function in one of the modes that is either in read/write or hold state. 3×3 Fredkin gate and Peres gate is used to perform the search line and match line operation. The design is verified and simulated by using Xilinx ISE simulator. The practical realization of reversible TCAM based chip will definitely reduce the power consumption of the network switches.



CONCLUSION & FUTURE SCOPE

In this project, have introduced an efficient QC novel architecture of (2ix j) Reversible RAM array module using proposed Feynman-gate, RDFF, and Reversible (i x 2i) decoder. The architecture of RRAM-Array module was performed under Xilinx-

2022.2 Vivado, the VHDL coding language. The simulation design and analytical outcomes obtained from waveforms were testified for memory functionality of RAM. The proposed RRAM module plays significant role in the field of reversible logics to study further for the designing and development of S-RAM array & D-RAM array for their application in FPGA kit.

Computers are intrinsically probabilistic machines, constrained by reliability of their algorithms and component parts. They throw away millions of bits, billions of times every second. They are based on irreversible logic devices, which have been recognized as being fundamentally energy inefficient for several decades. Truly, the only way we might ever get around this limit is by using reversible computing for the nano-scaled devices. Synthesis of more parity-reserving reversible circuits with less hardware along with full adders are now being developed and studied.

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