International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

A High-Gain DC-DC Converter featuring Progressive Gain for Fuel Cell Vehicles in Automobiles

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Abstract: For fuel cell vehicles, the DC-DC converter should have a high gain, low voltage stress, small size, and high efficiency. Conventional two-level, three-level, and cascaded boost converters, on the other hand, are unable to match the requirements. This work proposes a new non-isolated DC-DC converter with switched-capacitor and switched-inductor, which has a high gain, a wide input voltage range, low voltage stresses between components, and a common ground topology. The operating principle, component parameter design, and comparisons with other high-gain converters are all discussed in this paper. To obtain the dynamic model of the converter, the state-space averaging method and small-signal modeling method are used. Finally, simulation and experimental data back-up the proposed topology's usefulness. The experimental prototype's input voltage varies from 25 to 80 volts. The rated output voltage is 200V, with a 100W rated power. Under the rated state, the maximum efficiency is 93.1 percent. Fuel cell vehicles can use the suggested converter.
Keywords: DC-DC converter, Cascaded boost converters, Switched-capacitor, Fuel cell vehicle.

I. INTRODUCTION

The development of the transportation industry plays a vital role in the national economy. However, an increase in the number of fuel vehicles not only consumes a large amount of oil resources, but also causes serious environmental pollution problems. Therefore, all countries turn their attention to clean energy. The development of the new energy vehicle industry provides new ideas to solve these problems. Fuel cell vehicles have become a very promising development direction in the new energy vehicle industry due to its advantages of zero emissions, no pollution and high efficiency. The typical system structure of a fuel cell vehicle is shown in Fig.1 The low output voltage of the fuel cell makes it difficult to meet the demand of DC bus voltage in front of the inverter. Moreover, the fuel cell has a "soft" output voltage characteristic, i.e., the output voltage drops too fast with the increase of the output current. Therefore, the DC-DC converter with high-gain, wide input voltage range and small size should be applied to fuel cell vehicles to raise the fuel cell voltage to a higher voltage level and ensure the stability of the DC bus voltage.

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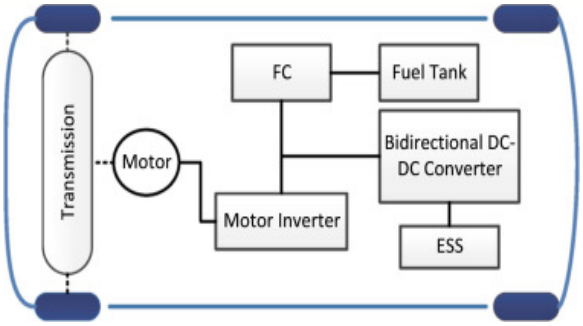

Fig.1 The typical system structure of a fuel cell vehicle

Isolated DC–DC converter can easily achieve high–gain by changing the transformer turns ratio. However, due to the leakage inductance of the transformer, the circuit will produce a peak voltage, which is easy to break down the devices in the circuit. The leakage inductance can also reduce the efficiency of the converter and cause electromagnetic interference problems. In addition, the transformer in the isolated converter also increases the size of the converter. Considering the size, cost and efficiency, the non–isolated DC–DC converter is more suitable for fuel cell vehicles. The traditional boost DC–DC converter is still used in many applications because of the small number of components and simple structure. The theoretical voltage gain of the boost converter is 1/(1–d), where d is the duty cycle of the drive voltage for the power switch.

However, the voltage gain is limited due to the parasitic parameters of the actual circuit and components. The voltage stresses across components in the circuit are also high, which needs more expensive high-voltage components, resulting in increased size and cost. In addition, there is an extreme duty cycle in traditional boost converters when achieving high-gain, which causes serious diode reverse recovery problems, resulting in increased losses. In terms of these disadvantages, conventional boost converters are not suitable for fuel cell vehicles.

The cascaded boost converter can achieve high–gain and wide input voltage range by sacrificing the overall power density and efficiency of the converter, but the voltage stresses across components are high and the circuit structures are complex. The boost three–level DC–DC converter can reduce the voltage stresses across components, but the voltage gain is still as low as the conventional boost converter. The voltage stresses across components are significantly reduced and the theoretical voltage gain can reach (1+d)/(1–d), which is slightly larger than the conventional boost converter. However, the voltage gain is still not enough for fuel cell vehicles. Z–source and quasi–Z–source networks are applied to the DC–DC converter to obtain the high–gain, but the voltage stresses of components in the converter are

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still high. A converter based on a series structure of three Z-source networks is proposed, which can obtain high-gain, wide input voltage range and low stress.

However, there are too many inductors and power semiconductors in the circuit, which increases the cost and size of the converter. The converters proposed can achieve high-gain and low voltage stress, but there is a non-common ground structure between the input and output ports of each converter. When the converter is working, there is a high frequency pulsated voltage between the input and output ports, which can cause serious EMI problems. In addition, the main problem is about the voltage feedback for the non-common ground structure. An isolated voltage feedback should be adopted, such as: linear optocoupler, which can increase the complexity of the sampling circuit.

The multi-level converters proposed can achieve high-gain and low voltage stresses across components. However, there are too many power semiconductors in the circuit, resulting in increased cost and size. Multiple power switches also increase complexity to the drive circuit and control strategy. The non-isolated converters with coupled-inductors proposed can easily achieve high-gain, reduce the size of the inductor and increase the power density of the converter. However, due to the existence of leakage inductance, additional clamp circuit or absorption circuit should be adopted to absorb the leakage inductance energy, which increases the complexity of the converter.

In this project, a DC-DC converter based on switched-capacitor and switched-inductor is proposed. The converter can obtain high-gain, wide input voltage range, low voltage stress and common ground structure between input and output ports. In addition, there is no extreme duty cycle and the power switches need only one PWM drive signal in circuit topology.

II PRINCIPLE OF THE PROPOSED CONVERTER

Configuration of the Proposed Converter

The circuit topology of the proposed converter is shown in Fig. 2. U_{in} and U_O are the input voltage and output voltage respectively. RL is the load resistance. The converter consists of two power switches (Q1, Q2), five diodes (D1-D5), four capacitors (C1-C4) and an inductor L. Q1 and Q2 are turned on and off simultaneously by using the same gate drive signal S.

When power switches Q1 and Q2 are turned on, S=1, and vice versa, calling S=0.

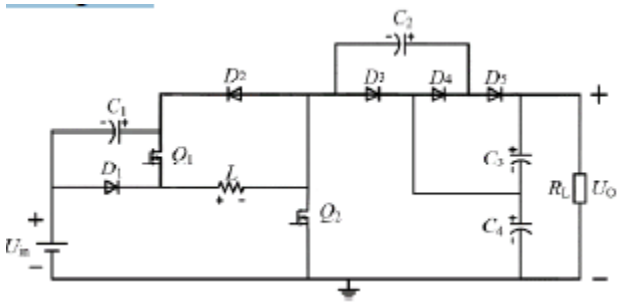

Fig. 2. The circuit topology of the proposed converter

Operating Principle of The Proposed

In order to analyze the proposed converter topology, some assumptions are made as follows:

a) The forward voltage drop of the diode and the on-state resistance of the power switch are ignored. The equivalent series resistances of inductors and capacitors are equal to 0.

b) The inductor is large enough in order to ensure that the circuit works normally. The capacitors are large enough in order to ensure that the voltage ripple of capacitors meets the requirements in this project. In this project, the operating principle in Continuous Conduction Mode (CCM) is

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analyzed. The key operating waveforms of the proposed converter in CCM are shown in Fig. 3 According to the switching states of power switches, there are two operating states for the proposed converter, as shown in Fig.4.

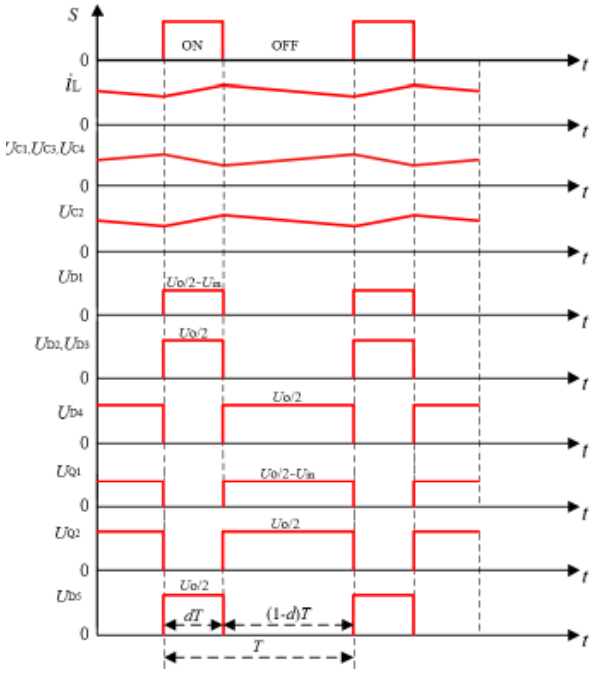

Fig. 3. The key operating waveforms of proposed converter in CCM

When power switches Q1 and Q2 are turned on (S=1), the equivalent circuit is shown in Fig. 4(a), defined as the ON state. The diodes D1, D2, D3, D5 are reverse biased and three current loops appear in the circuit. U_{in} and C_1 charge the inductor L through Q_1 and Q_2. Capacitor C_4 charges the capacitor C2 through power switch Q_2 and diode D_4. The series part of the capacitors C3 and C4 transfers energy to the load RL.

When power switches Q1 and Q2 are turned off (S=0), the equivalent circuit is shown in Fig. 4(b), defined as the OFF state. The diode D4 is reverse biased and four current loops appear in the circuit. Inductor L charges capacitor C1 through D1 and D2. Uin and L charge capacitor C4 through D1 and D3. Uin, L and C2 charge the series part of C3 and C4 through the diodes D1 and D5. The series part of the capacitors C3 and C4 still transfers energy to the load RL.

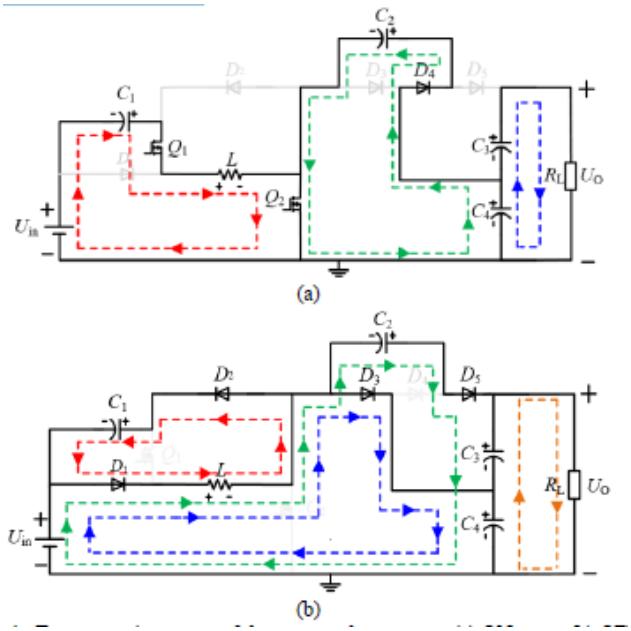

Fig. 4. Two operating states of the proposed converter (a) ON state. (b) OFF state

Analysis of Voltage Gain and Voltage Stress

Equations (17) and (18) can be obtained by applying Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) to the circuit topology in Fig. 4(a).$\{U_{L(ON)} = U_{in} + U_{C1}\ U_{C2} = U_{C4}\ U_O = U_{C3} + U_{C4}$

(17)

where U_{C1}, U_{C2}, U_{C3} and U_{C4} are the capacitor voltages across C1, C2, C3 and C4 respectively. UL(ON) is the inductor voltage across L when the converter operates in the ON state. UO is the output voltage of the converter.$\{IC1(ON) = -I_L\ IC2(ON) = IC3(ON) - IC4(ON)\ IC3(ON) = -Io$

(18)

where I_L is the average current of inductor L. $I_{C1(ON)}$, $I_{C2(ON)}$, $I_{C3(ON)}$, and $I_{C4(ON)}$ are the average currents of the capacitors C1, C2, C3 and C4 respectively, when the converter operates in ON state. I_O is the load current. Equations (19) and (20) can be obtained by

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ISSN: 2457-0362

applying KVL and KCL to the circuit topology in Fig. 4(b)

$$\{U_{LOFF} = -U_{Cl1}\, U_{C4} = U_{in} - U_{L(OFF)}$$

$$U_0 = U_{in} - U_{L(OFF)} + U_{C2}\, U_0 = U_{C3} + U_{C4} \quad (19)$$

$$\{U_{L(OFP)} = -U_{Cl1}\, U_{C4} = U_{in} - U_{L(OFF)}$$

$$U_0 = U_{in} - U_{L(OFF)} + U_{C2}\, U_0 = U_{C3} + U_{C4} \quad (20)$$

where $U_{L(OFF)}$ is the inductor voltage across L when the converter operates in the OFF state.

$$\{I_{C1(OFF)} = I_L + I_{C2(OFF)} + I_{C3(OFF)} - I_{C4(OFF)}$$

$$I_{C2(OFF)} = -I_0 - I_{C3(OFF)} \quad (21)$$

Where $I_{C1(OFF)}$, $I_{C2(OFF)}$, $I_{C3(OFF)}$, and $I_{C4(OFF)}$ are the average currents of the capacitors C1, C2, C3 and C4 respectively, when the converter operates in the OFF state. Equation (22) can be obtained by applying the voltage-second balance principle to inductor L, and equation (23) can be obtained by applying the ampere-second balance principle to capacitors C1, C2, C3 and C4.

$$U_{LON} \times dT + U_{L(OFF)} \times (1-d)T = 0 \quad (22)$$

$$I_{Cl(ON)} \times dT + I_{Cl(OFF)} \times (1-d)T = 0$$

$$I_{C2(ON)} \times dT + I_{C2(OFF)} \times (1-d)T = 0$$

$$I_{C(ON)} \times dT + I_{C3(OFF)} \times (1-d)T = 0 \quad (23)$$

$$I_{C4(ON)} \times dT + I_{C4(OFF)} \times (1-d)T = 0$$

where d is the duty cycle of power switches Q1 and Q2. T is the switching period. In terms of (18), (20) and (22), the theoretical voltage gain M of the converter can be obtained.

$$M = \frac{U_0}{U_{in}} = \frac{2(1-d)}{1-2d} \quad (24)$$

where 0<d<0.5. The proposed converter cannot work normally if d>0.5. In terms of (18), (20), (22) and Fig. 4, the voltage stresses across all capacitors and power semiconductors in the circuit topology are obtained as shown in (24).

$$U_{C1} = U_{D1} = U_{Q1} = U_0/2 - U_{in}$$

$$U_{C2} = U_{C3} = U_{C4} = U_0/2 \quad (24)$$

$$U_{D2} = U_{D3} = U_{D4} = U_{D5} = U_0/2$$

$$U_{Q2} = U_0/2$$

From (23), the converter can obtain a high-gain and the duty cycle d is always less than 0.5 without extreme duty cycles. From (24), the voltage stresses of all capacitors and power semiconductors in the circuit topology are no more than $U_O/2$, which is beneficial to reducing size, cost and improving efficiency of the converter. Assuming that the input power of the converter is equal to the output power in the ideal state, equation (25) can be obtained.

$$U_m \times I_m = U_0 \times I_0 \quad (25)$$

where I_{in} is the average input current of the converter. In terms of (19), (21), (23), (25) and Fig. 5, the inductor current I_L is obtained as shown in (26) and the current stresses of all capacitors in the circuit topology are obtained as shown in (27).

$$I_L = \frac{2}{1-2d} I_0 \quad (26)$$

$$IC1(ON) = \frac{-2}{1-2d} I_0$$

$$I_{C1(OFF)} = \frac{2d}{(1-2d)(1-d)} I_0$$

$$I_{C2(ON)} = \frac{1}{d} I_0$$

$$I_{C2(OFF)} = \frac{-1}{1-d} I_0$$

$$I_{C3(ON)} = -I_0$$

$$(27) I_{C3(OFF)} = \frac{d}{1-d} I_0$$

$$I_{C4(ON)} = -\left(1 + \frac{1}{d}\right) I_0$$

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$$I_{C4(OFF)} = \frac{1+d}{1-d} I_0$$

In terms of (10), (11) and Fig.5, the current stresses of all power semiconductors are obtained as shown in (28).

$$I_{Q1} = I_{D1} = -I_{Cl}(ON) = \frac{2}{1-2d} I_0$$

$$I_{Q2} = I_L + I_{C2(ON)} = \frac{1}{d(1-2d)} I_0$$

$$I_{D2} = -I_{Cl(OFF)} = \frac{-2d}{(1-d)(1-2d)} I_0 \qquad (28)$$

$$I_{D3} = I_{44(OFF)} - I_{C3(OFF)} = \frac{1}{1-d} I_0$$

$$I_{D4} = I_{C2(ON)} = \frac{1}{d} I_0$$

$$I_{D5} = I_0 + I_{C3(OFF)} = \frac{1}{1-d} I_0$$

The MOSFET is adopted as a power switch in an experimental prototype of the proposed converter. Because the MOSFET and Schottky diode are suitable for low voltage and large current applications, this project is only concerned with the voltage stresses of the components. The current stresses of the components are only used as an auxiliary reference for later component selection.

Comparison With Other Converters

The proposed converter is compared with other converters in terms of voltage gain, voltage stress, the number of components, and common ground structure, as shown in Table I. The relationships between voltage gain M and duty cycle d among different converters are shown in Fig.3.9. Compared with conventional boost converters, the proposed converter can obtain a higher gain. When the proposed converter achieves high-gain, the duty cycle is always less than 0.5 without an extreme duty cycle. Furthermore, the voltage stresses across components of the proposed converter are no more than $U_O/2$, rather than the UP of a conventional boost converter. The low voltage-stress can reduce the volume and cost of the capacitors, which occupy a large volume of the converter. The low voltage-stress can also reduce the voltage breakdown risk of the device and improve the reliability of the converter.

Two converters for fuel cell vehicles are proposed in [28] and [29] with low voltage stress and wide input voltage range. The voltage stresses across all components are reduced to Uo/2 and the voltage gain ($M = 2/(1-d)$) is two times better than the conventional boost converter. But the voltage gain is lower than that of the proposed converter in this project, and these two converters may suffer from extreme duty cycles when high-gain is achieved. Furthermore, the circuit topologies are uncommon in ground structure and there is a potential difference equal to $U_o/2$ between the input and output ports in each converter, which can cause safety. Although this potential difference is not a high frequency pulsated voltage, the non-common ground structure also brings difficulty to the sampling of the output voltage. The converter in [30] can obtain low voltage stresses across components and the operating range of d is from 0.5 to 0.75. However, the voltage gain is still low and there is an extra inductor in circuit topology compared with the proposed converter in this project.

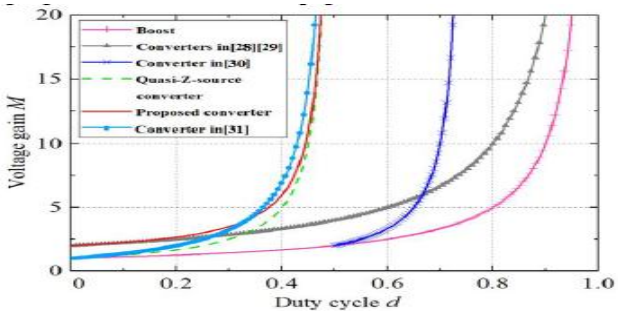

Fig. 5. Relationships between voltage gain M and duty cycle d among different converters.

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Compared with the traditional quasi- Z- source converter ($M = 1/(1 - 2d)$), the voltage gain of the proposed converter ($M = 2(1-d)/(1-2d)$) is always larger than that of the traditional quasi- Z-source converter within $0 < d < 0.5$ and the smaller d is,Compared with the traditional quasi- Z-source converter ($M = 1/(1-2d)$), the voltage gain of the proposed converter ($M = 2(1-d)/(1-2d)$) is always larger than that of the traditional quasi- Z-source converter within $0 < d < 0.5$ and the smaller it is, the greater voltage gain difference is. The voltage stresses across components of the proposed converter are no m more than $U_0/2$, rather than the UO of the quasi-Z-source converter.

The voltage gain of the converter is slightly greater than that of the proposed converter within $0.33 < d < 0.5$ and is smaller than that of the proposed converter within $0 < d \leq 0.33$. But the voltage gain of the proposed converter in this project can meet the requirements of high- gain for fuel cell vehicles. In addition, the converter adopts a large number of inductors, which increases the size of the converter.

The circuit topology is a non-common ground structure and there is a high frequency pulsated voltage between the input and output ports, which results in an EMI problem. The proposed converter can obtain high-gain, low voltage stresses across components. The common ground structure of the proposed converter can also avoid EMI problems. In addition, the power switches can be driven by only one PWM driving signal, which is beneficial to reducing the complexity of driving circuits. By using a switched capacitor technique, there should be an inrush current when the converter works at hard switching conditions. This problem can be suppressed by reducing the voltage differential between two capacitors, which can be achieved by increasing the switching frequency. Besides, the soft switching technique can also effectively suppress the EMI and inrush current caused by the switched capacitor technique. Based on the comparison results among different converters, the proposed converter in this project is more advantageous in terms of high-gain, wide input voltage range, low voltage stress and common ground structure.

III. PARAMETERS DESIGN AND DYNAMIC MODELING

In terms of the converter topology, the inductor L can be calculated by (13).

$$\mathcal{L} = u\mathcal{L} \frac{dt}{di_{\mathcal{L}}} \quad (13)$$

The maximum inductor current and the maximum duty ratio can be obtained when the input voltage is the lowest, that is U_{in}=25V in the proposed converter. Therefore, the inductor is designed when U_{in}=25V, U_O=200V, f=20kHz and RL=400Ω in this project. Assuming the current ripple of inductor L isΔI_L , hence, the current ripple coefficient of inductor L is $\gamma = \Delta I_L / I_L$. In order to avoid excessive inductor current ripple, the ripple rate of inductor current is set as $\gamma \leq 0.4$. When the converter operates in the ON state as shown in Fig. 4(a), $u_L = u_{in} + uc1$, $dt = d \times T = d/f$. In the calculation equation of inductance can be obtained as (14).

$$L \geq \frac{d'(1-2d')R_L}{4\gamma f} = 750\mu H \quad (14)$$

Where f is the switching frequency of the converter and d is the duty cycle of the drive signal for power switches Q1 and Q2. When R_L=400Ω and U_O=200V, the output current $I_O = U_O / R_L$ =0.5A, I_L=7.14A can be obtained. When U_{in}=25V and U_O=200V, the peak value of inductor current I_{L_peak} is obtained in equation 15.

$$I_{L\_peak} = I_L + \frac{\Delta L}{2} = I_L + \frac{I_L \gamma}{2} = 8.6A \quad (15)$$

The energy storage of the magnetic core is calculated as in (4).

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$L.I^2_{L\_peak} = 0.8\,mH \times (8.6)^2 = 59.8\text{mH.A}^2$ (16)

Considering the flux density and price, the ferrosilicon aluminum magnetic core is adopted in this project. By referring to magnetic core selection curves of Magnetics company for the iron-silica-aluminum, the 77438 magnetic core is selected for inductor design in this project. The capacitor C can be calculated by using (16). Assuming the voltage ripples of capacitors C1, C2, C3, C4 are $f'U_{C1}$, $f'U_{C2}$, $f'U_{C3}$, $f'U_{C4}$, respectively. In the calculation equation of capacitance can be obtained as (6\17).

$$C = ic\frac{dt}{duc} \quad (17)$$

$$\begin{cases} C_1 = \dfrac{2dIo}{(1-2d)\Delta U_{C1} f} \\ C_2 = \dfrac{Io}{\Delta U_{C2} f} \\ C_3 = \dfrac{dIo}{\Delta U_{C3} f} \\ C_4 = \dfrac{(1+d)Io}{\Delta U_{C4} f} \end{cases} \quad (18)$$

5.2. Dynamic Modeling Analysis

When the converter operates in the ON state, capacitors C2 and C4 are in parallel as shown. The relationship between C2 and C4 is shown in (7), indicating that there is an invalid variable between C2 and C4.

$$C_2\frac{duc_2}{dt} = -C_4\frac{duc_4}{dt} \quad (7)$$

In order to eliminate the invalid variable between C2 and C4, the series equivalent resistance r1 is introduced into C2 and C4 loop and equation (7) can be written as (8).

$$C_2\frac{duc_2}{dt} = -\frac{uc_4 - uc_2}{r_1} \quad (8)$$

Where the r1 is the equivalent series resistance in C2 and C4 loop, defined as r1 = 0.01Ω. When the converter operates in the OFF state, the series equivalent resistance r2 = 0.01Ω is adopted to eliminate the invalid variable of C1, C2, C3 and C4 loops as shown in Fig. 4(b). After adopting equivalent resistances r1 and r1, the equivalent circuit topology is as shown in Fig.6.

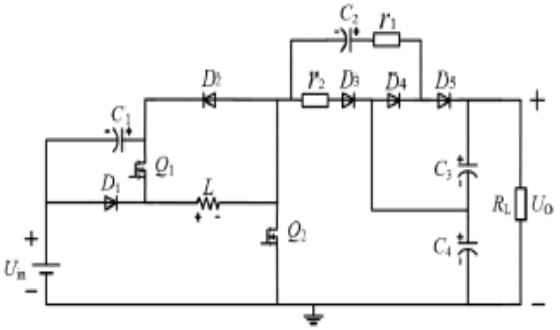

Fig. 6. Circuit topology after adopting equivalent resistances r1 and r2

The state-space averaging method is used to model the converter in CCM. uin(t) is the input variable, uo(t) is the output variable and d(t) is the control variable. iL(t), uC1(t), uC2(t), uC3(t), uC4(t) are the state variables of inductor L and capacitors C1, C2, C3, C4 respectively. When the converter operates in the ON state and the working time is dT, the state space equation is obtained as (21). When the converter operates in the OFF state and the working time is (1-d)T, the state space equation is obtained as (22). In terms of (21) and (22), the state space averaging equation over a switching period can be obtained as shown in (23). Equation (24) is obtained when all variables are written as the sum of DC and small signals components. By substituting (24)

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into (23) and removing the DC components, the small signal model of the converter is obtained as shown in (25).

$$\begin{cases} i_L(t)=I_L+\tilde{i}_L(t) \\ u_{C1}(t)=U_{C1}+\tilde{u}_{C1}(t) \\ u_{C2}(t)=U_{C2}+\tilde{u}_{C2}(t) \\ u_{C3}(t)=U_{C3}+\tilde{u}_{C3}(t) \\ u_{C4}(t)=U_{C4}+\tilde{u}_{C4}(t) \\ u_{in}(t)=U_{in}+\tilde{u}_{in}(t) \\ u_o(t)=U_o+\tilde{u}_o(t) \\ d(t)=D+\tilde{d}(t) \end{cases} \quad (24)$$

where IL, UC1, UC2, UC3, UC4, Uin, UO, D are the DC steady-state components of the corresponding variables. iL(t) uC1(t) uC2(t) uC3(t) uC4(t) uin(t) uO(t) d(t) are the small signal components of the corresponding variables.

TABLE I DESIGN PARAMETERS OF THE CONVERTER

Parameters	**Values**
Rated power P	100W
Input voltage U_{in}	25V-80 V
Rated output Voltage U_0	200V
Rated load resistance R_L	400Ω
Switching frequency f	20kHz
Inductor L	800μH
Capacitors C_1,C_2,C_3,C_4	470μF
Power switches Q_1,Q_2	DXTK102N30P
Diodes D_1,D_2,D_3,D_4,D_5	DSEC 60-03A

The design parameters of the converter are shown in Table I. When Uin=25V and UO=200V, in terms of (25) and Table II, the transfer functions of control-to-output are obtained as shown in equation (26). The dynamic model of the proposed converter in (26) is written into the pole-zero form as shown in (27). In order to simplify analysis, the original model in (27) is reduced from 5 to 4 in order to obtain the simplified model in (28). By appropriate pole-zero elimination method, the (s+3.135×105) in numerator and the (s+4.283 ×105) in denominator are eliminated in equation(27). The BODE diagram curves of (27) and (28) are shown in Figure 7. From Fig.7, it can be seen that the original and simplified model curves are approximately the same. Therefore, the PI controller is designed based on (28).

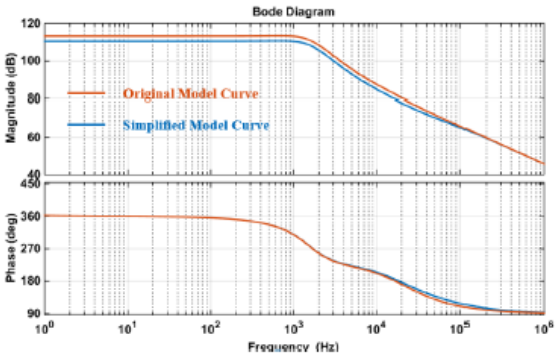

Fig.7. Bode diagram of the proposed converter.

The PI controller is designed in order to achieve stable operation for the converter system. The block diagram of the closed-loop control system for the converter is shown in Fig.8. GFB(s) is the feedback network transfer function. The actual prototype adopts the Hall sensor to collect the output voltage. Gd uo(s) is the transfer function of the converter from control to output. GPI(s) is the transfer function of the PI controller as shown in (29). The converter system can obtain good dynamic and static performance by using the PI controller.

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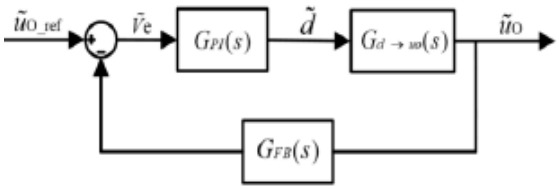

Fig.8. The block diagram of the closed-loop control system of the converter

$$G_{ZPK}(s)=\frac{-1.2247\times10^{9}(s+3.135\times10^{5})(s-1.307\times10^{5})(s+3.031\times10^{4})(s-0.007247)}{(s+4.283\times10^{5})(s+1.165\times10^{5})(s+0.2883)(s^{2}+1.242\times10^{4}s+9.04\times10^{7})}$$

$$\hat{G}_{ZPK}(s)=\frac{-1.2247\times10^{9}(s-1.307\times10^{5})(s+3.031\times10^{4})(s-0.007247)}{(s+1.165\times10^{5})(s+0.2883)(s^{2}+1.242\times10^{4}s+9.04\times10^{7})}$$

$$G_{PI}(s)=K_P+\frac{K_I}{s} \qquad (29)$$

where the KP is the proportional coefficient and KI is the integral coefficient. For this work, Kp = 0.000008 and KI = 0.000005. By using the PI controller, the Bode diagram of the converter closed-loop system is shown in Fig.9. The phase margin of the closed-loop system is 54°, which indicates the system can achieve stable operation.

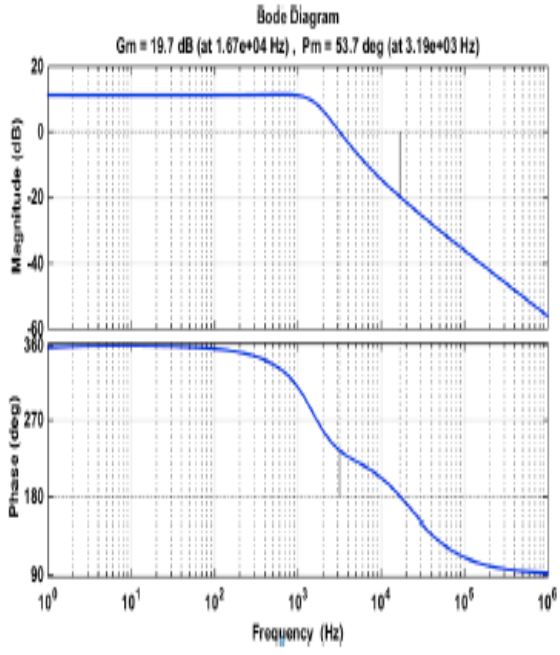

Fig. 9. The BODE diagram of a closed-loop system for the converter.

In terms of practicality and stability, the bilinear transformation method is adopted to design the digital controller in this project. By using bilinear transformation method, the relation between variable s in s domain and variable z in z domain is shown in (30) as follows [32].

$$s=\frac{2}{T_s}\cdot\frac{z-1}{z+1} \qquad (30)$$

where Ts is the sampling period of a discrete system. Ts= 0.00005s in this project. In terms of (29) and (30) above, by using bilinear transformation method, the PI controller equation in z domain is obtained as (31).

$$\frac{d(z)}{Ve(z)}=\frac{(K_P+\frac{T_s}{2}\cdot K_I)\cdot z+\frac{T_s}{2}\cdot K_I-K_P}{z-1} \qquad (31)$$

where Ve(z) is the input error voltage of the PI controller in the z domain. d(z) is the output duty cycle of the PI controller in the z domain. The values of KI, KP and Ts above are substituted into equation (31) to obtain (32) as follows.

$$\frac{d(z)}{Ve(z)}=\frac{8\times10^{-6}+7.99\times10^{-6}\cdot z^{-1}}{1-z^{-1}} \qquad (32)$$

Equation (32) is transformed into the difference equation as shown in (33), which is the expression of the discrete PI controller. According to (33), a PI control program can be written in a controller to realize closed-loop control and ensure the stability of the converter system.

$$d(k)=d(k-1)+8\times10^{-6}\cdot Ve(k)+7.99\times10^{-6}\cdot Ve(k-1) \quad (33)$$

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Simulation results of converter during Drive voltage and Load current

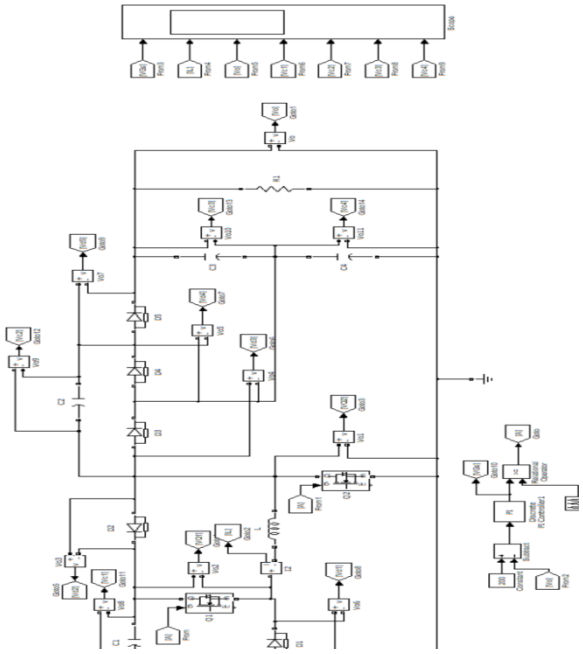

Fig.10. Simulation results of converter during Drive voltage and Load current

In order to verify the effectiveness of the proposed converter, a simulation model is built for the converter system and simulation parameters are shown in Table I. When the input voltage is U_{in}=25 V and the reference output voltage is set as U_{O_ref} =200 V, the simulation results are shown in Fig.10.

From Fig10 and fig 11, the inductor current IL is 7.5 A, which is consistent with the theoretical calculation result. The output voltage U_O has been stable at 200 V. The voltage stresses across all capacitors and power semiconductors are as follows: U_{Q1}=U_{C1} =U_{D1} ≈ 75 V U_{Q2} =U_{C2} =U_{C3} =U_{C4} =U_{D2} =U_{D3} =U_{D4}=U_{D5} ≈ 100 V, which are consistent with the theoretical calculation results obtained.

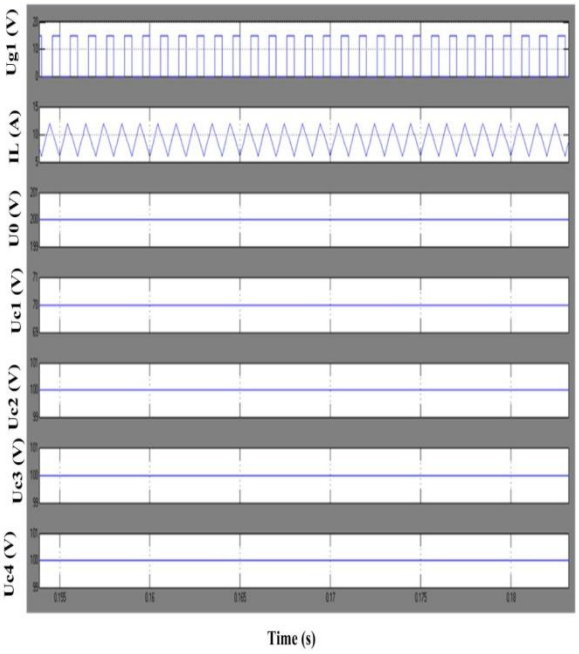

Fig.11. Simulation results of converter during Drive voltage Ugs, inductor current I_L, output voltage U_O and voltage stresses across C1, C2, C3, C4.

The simulation results show that the proposed converter has advantages of high-gain and low voltage stresses across components, which verifies the effectiveness of the circuit topology. The dynamic simulation results of the converter are shown in Figure 10. When the simulation time is 1s, the input voltage of the converter Uin starts to drop from 60V and finally drops to 25V, with a total time of 14s. When the simulation time is 16s, the output current IO changes suddenly from 250mA to 500mA and remains 200ms. Then the IO changes suddenly from 500mA to 250mA. From Fig.12, it can be concluded that the converter can maintain the output voltage stable around the reference voltage under the input voltage and load disturbance. The system can obtain a good anti-interference performance.

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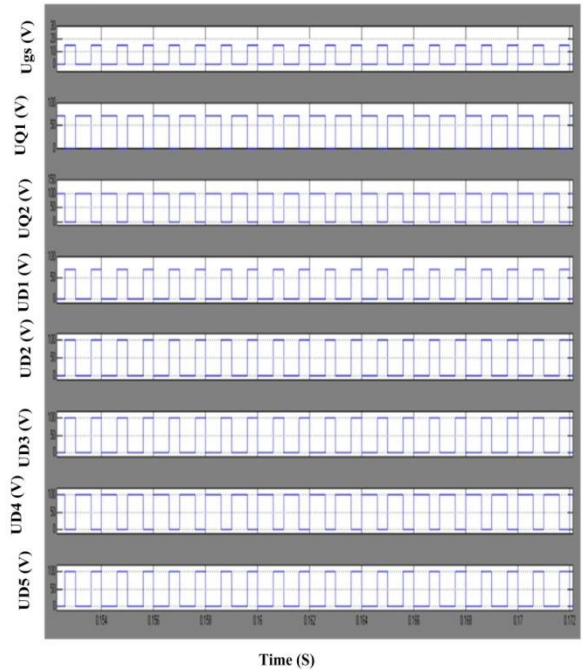

Fig.12. Simulation results of converter during Drive voltage U_{gs}, voltage stresses across Q1 and Q2, voltage stresses across D1, D2, D3, D4, D5.

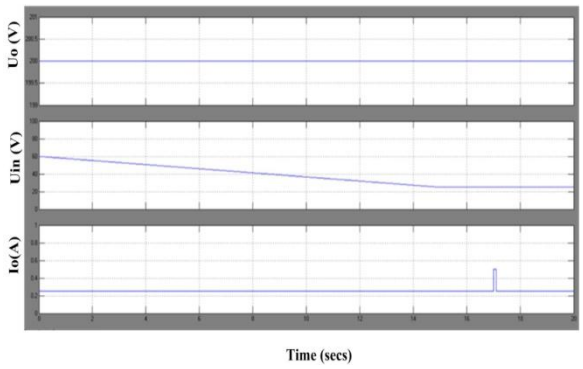

Fig.13. Simulation results of the converter under the input voltage disturbance and load disturbance.

IV. CONCLUSION

This project presents a non-isolated DC-DC converter topology for fuel cell vehicles. The proposed converter can obtain high-gain and wide input voltage range. The voltage gain can reach 2(1-d)/(1-2d) and duty cycle d<0.5 while achieving high-gain. The voltage stresses across components are less than half of the output voltage, which is beneficial to reduce the size and cost of the converter. In addition, the circuit topology is a common ground structure, which can avoid EMI and safety problems. The converter can always maintain the stability of the output voltage by closed-loop control. There is no voltage overshoot and impulse current during the soft-start process by adopting the soft-start program. Under the rated state, the measured maximum efficiency of the prototype is 93.1%. The proposed converter is suitable for fuel cell vehicles.

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