International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

Design of CDMA Encoder and Decoder using Standard Basis and Walsh Codes

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ABSTRACT

The rapid evolution of communication systems demands efficient and robust encoding and decoding techniques. This paper addresses the design of Code Division Multiple Access (CDMA) Encoder and Decoder using both Standard Basis and Walsh Codes. In the introduction, we discuss the increasing need for advanced communication systems and the pivotal role of CDMA in meeting these demands. The conventional CDMA systems primarily employ Standard Basis for encoding, which, although effective, faces certain drawbacks such as limited capacity and vulnerability to interference. In this context, the proposed system introduces the integration of Walsh Codes, a set of orthogonal codes, into the CDMA encoding and decoding process. This enhancement aims to mitigate the limitations of the conventional system by providing increased capacity, improved signal separation, and enhanced resistance to interference. The works details the design and implementation of the proposed CDMA Encoder and Decoder, highlighting its potential to significantly improve the performance and reliability of communication systems in the ever-evolving technological landscape.

Keywords: encoder,decoder,walsh codes,cdma.

1. INTRODUCTION

ON-CHIP interchanges significantly affect the general zone, execution, and power utilization of present day framework on-chips (SoCs). Expanding the correspondence over-head debases the speedup accomplished by parallel figuring as per Amdahl's law [1]. In this manner, creating effi-cient superior on-chip interconnects has been of central significance for the parallel and elite figuring advances. Systems on-chips (NoCs) are the most versatile interconnection worldview that is equipped for tending to different application needs and meet distinctive perfor-mance prerequisites of substantial remaining tasks at hand [2], including inertness by means of versatile directing [3], throughput by means of enhanced way jumper sity [4], control dispersal by streamlining the NoC to focused outstanding tasks at hand [5], and adaptability by run-time design [6]. In NoCs, information are dealt with as parcels, while on-chip handling components (PEs) are considered as system hubs between associated by means of switches and switches. NoCs give an adaptable asumption and vast asset overheads [7]. The NoC layering model parts the exchange into four layers: 1) application;transport; 3) system; and 4) physical layers [8]. A crossbar is the fundamental building square of the NoC physical layer. A cross-bar switch is a common correspondence medium receiving a numerous entrance procedure to empower physical bundle trade. The fundamental asset sharing systems embraced by existing NoC crossbars are time-division various access (TDMA), where the physical connection is time shared between the intercon-

nected PEs [9], and space-division different access (SDMA), where a committed connection is built up between each match of interconnected PEs [10]. The physical layer of a NoC switch likewise contains buffering and capacity gadgets [7].CDMA is another medium sharing method that use the code space to empower concurrent medium access. In CDMA channels, each transmit– get (TX-RX) combine is allocated an exceptional bipo-lar spreading code and information spread from all transmitters are summed in an added substance correspondence channel.The spreading codes in established CDMA frameworks are symmetrical—cross relationship between's symmetrical codes is zero—which empowers the CDMA beneficiary to appropriately disentangle the got entirety through a correlator decoder. Traditional CDMA frameworks depend on Walsh– Hadamard symmetrical codes to empower medium sharing. CDMA has been proposed as an on-chip intercon-nect sharing method for both transport and NoC interconnect models [11]. Numerous focal points of utilizing CDMA for on-chip interconnects incorporate lessened power utilization, settled correspondence idleness, and decreased framework complex-ity [12]. A CDMA switch has less wiring many-sided quality than a SDMA crossbar and less intervention overhead than a TDMA switch, and in this manner gives a decent trade off of both. Be that as it may, just essential highlights of the CDMA innovation have been investigated in the on-chip interconnect writing.Over-burden CDMA is an outstanding medium access method conveyed in remote interchanges where the quantity of clients sharing the correspondence channel is helped by expanding the quantity of usable spreading codes to the detriment of expanding numerous entrance obstruction (MAI) [13]. The over-burden CDMA idea can be connected to on-chip interconnects to build the interconnect limit.

2. LITERATURE SURVEY

Intra-chip correspondence is a noteworthy bottleneck in present day multiprocessor framework on-chip (MPSoC) outlines. The transport topology is the most well-known on-chip interconnect innovation and transport conflict in one of the significant issues in transport based MPSoC plans. Code division different access (CDMA) has been proposed as a transport sharing system to defeat the transport conflict issue. In CDMA, a predetermined number of symmetrical spreading codes can share the medium because of the Multiple Access Interference (MAI) issue. In remote interchanges, over-burden CDMA has been considered to expand the framework limit by including additional non-symmetrical spreading codes with particular qualities. We propose a novel CDMA transport design utilizing the over-burden CDMA ideas to expand the most extreme number of centers having the same CDMA transport in MPSoC by 25% at a negligible Improved Overloaded CDMA Interconnect (OCI) Bus Architecture for On-Chip Communication:

On-chip interconnect is a noteworthy building square and a principle execution bottleneck in current complex System-on-Chips (SoCs). The transport topology and its subsidiaries are the most sent correspondence structures in contemporary SoCs. Space exchanging exemplified by cross bars and multiplexers, and time sharing are the key empowering influences of different transport structures. The cross bar has quadratic multifaceted nature while asset sharing altogether debases the general framework's execution. In this work we rouse utilizing CDMA (CDMA) as a transport sharing methodology which offers numerous points of interest over other topologies. Our work looks to supplement the regular CDMA transport includes by applying over-burden CDMA practices to expand the transport usage effectiveness. We propose the Difference-Overloaded CDMA Interconnect (D-OCI) transport that use the adjusting Parallel over-burden CDMA interconnect (OCI) transport engineering for on-chip

interchanges On-chip interconnects are the execution bottleneck in present day System-on-Chips (SoCs).

Transport topologies and Networks-on-Chip (NoCs) are the fundamental methodologies used to actualize on-chip correspondence. The interconnect texture empowers asset sharing by Time or potentially Space Division Multiple Access (T/SDMA) strategies. CDMA (CDMA) has been proposed to empower asset partaking in on-chip interconnects where every datum bit is spread by a one of a kind symmetrical spreading code of length N. Not at all like T/SDMA, in remote CDMA, the correspondence channel limit can be expanded by defeating the Multiple Access Interference (MAI) issue. Accordingly, we present two over-burden CDMA interconnect (OCI) transport structures, in particular TDMA-OCI (T-OCI) and Parallel-OCI (P- OCI) to expand the traditional CDMA interconnect limit. We execute and approve

Systems on Chip (NoCs) have supplanted on-chip transports as the foremost correspondence methodology in vast scale Systems-on-Chips (SoCs). CDMA (CDMA) has been proposed as an interconnect texture that can accomplish high throughput and settled exchange inertness because of the CDMA transmission simultaneousness. Over-burden CDMA Interconnect (OCI) is a compositional development of the customary CDMA interconnects that can twofold their transfer speed at marginalcost. Utilizing OCI in CDMA-based NoCs has the capability of giving higher transfer speed at low-power and-territory overheads contrasted with otherNoC structures. Besides, settled idleness and unsurprising execution accomplished by the inalienable CDMA simultaneousness can lessen the exertion and overhead required to actualize QoS. In this work, we advance the Overloaded CDMA interconnect for Network on Chip

3. PROPSOED METHOD

3.1 Overall Structure of CDMA NoC

The basic structure of applying CDMA technique to NoC with a star topology is shown in Fig. 1. In this figure, a PE executes tasks of the application and network interface (NI) divides data flows from PE into packets and reconstruct data flows by using packets from NoC. In the sender, packet flits from NI are transformed to a sequential bit stream via a parallel-to-serial (P2S) module. This bit stream is encoded with an orthogonal code in the Encoding module (E in Fig. 1). The coded data from different encoding modules are added together in the Addition module (A in Fig. 1). Then, the sums of data chips are transmitted to receivers. In the receiver, Decoding modules (D in Fig. 1) reconstruct original data bits from the sums of data chips. Then these sequential bit streams are transformed to packet flits by serial-to-parallel (S2P) modules. Finally, these packet flits are transferred to NI. In the CDMA NoC, network scheduler receives the transmitting requests from senders and assigns proper spreading codes to the senders and requested receivers. Note that all-zero codeword is assigned to nodes having no data to transmit/ receive. Moreover, when there are multiple senders requesting the same receiver, the scheduler will apply an arbitration scheme, for example, round-robin. The chip counters calculate how many orthogonal chips are used in one encoding/decoding operation. Each node needs two chip counters, one for the sender and the other for the receiver. Note that packet flits from NI can also be transformed to multiple bit streams in the P2S module to make tradeoffs between power/area cost and packet transfer latency, and the scheduler should provide a bit-synchronous scheme to maintain the orthogonality of the transmitted channels, as discussed in [8]. In this brief, we focus on the design and comparison of WB- and SB-based CDMA encoding/decoding method, which corresponds to E, A, and D modules in Fig. 1.

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3.2 CDMA Encoder

Two different encoding methods, WB encoder and SB encoder, are compared in Fig. 2. Fig. 2(a) shows the WB encoder architecture. An original data bit is first encoded with a Walsh code by taking an XOR operation. Then, these encoded data are added up to a multibit sum signal by taking arithmetical additions. Each sender needs an XOR gate, and multiple wires are used to express the sum signal if we have two or more senders. Moreover, the number of wires increases as the number of senders increases. Fig. 2(b) shows our SB encoding scheme. An original data bit from a sender is fed into an AND gate in a chip-by-chip manner, and it will be spread to n-chip encoded data with an orthogonal code of a standard basis. The relationship between a bit and a chip is shown in Fig. 3. Then, the encoded data from different senders are mixed together through an XOR operation, and a binary sum signal is generated. Therefore, the output signal is always a sequence of binary signal transferred to destination using one single wire. The progressions of both the encoding schemes are depicted in Fig. 3. Fig. 3(a) and (b) illustrates the WB encoding process with four-chip Walsh codes and the SB encoding process with four-chip standard orthogonal codes, respectively

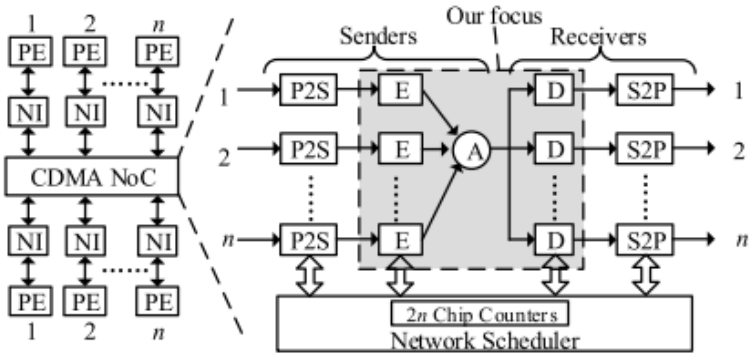

Figure 1. CDMA-NoC

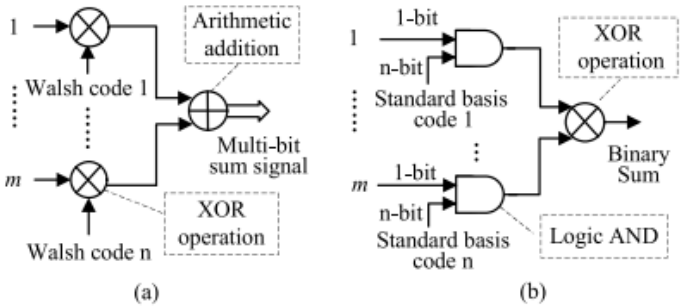

Fig. 2. Block diagram of encoding scheme. (a) WB encoder. (b) SB encoder.

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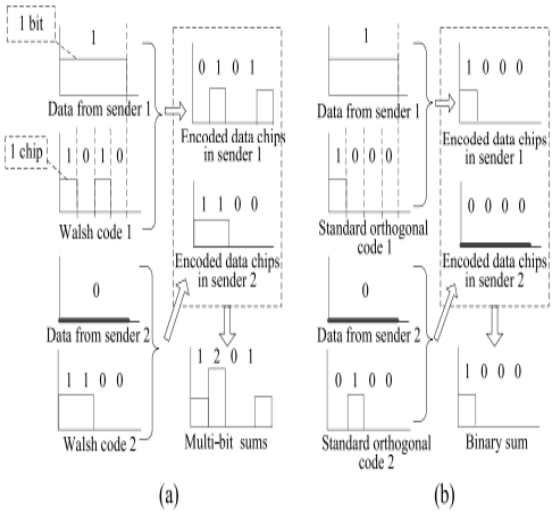

Fig. 3. Data encoding example. (a) WB encoding. (b) SB encoding.

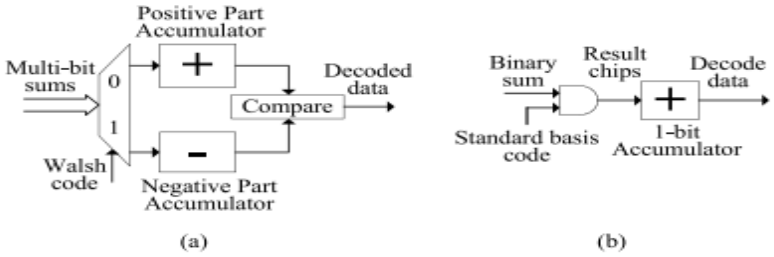

Fig. 4. Block diagram of decoding scheme. (a) WB encoder. (b) SB encoder.

3.4 CDMA Decoder

The WB decoding scheme is presented in Fig. 4(a). According to the chip value of Walsh code, the received multibit sums are accumulated into positive part (if the chip value is 0) or negative part (if the chip value is 1). Therefore, the two accumulators in the WB decoder separately contain a multibit adder to accumulate the coming chips and a group of registers to hold the accumulated value. Through the comparison module after the two accumulators, the original data is reconstructed. If the value of positive part is large, the original data is 1. Otherwise, the original data is 0. The SB decoding scheme is shown in Fig. 4(b). When the binary sum signal arrives at receivers, an AND operation is taken between the binary sum and the corresponding orthogonal code in chip-bychip manner. Then, the result chips are sent to an accumulator. After m-chips are accumulated (m is the length of the orthogonal code), the output value of the accumulator will be the corresponding original data. Note that there is always only one chip equal to 1 and all othechips are equal to 0 for an orthogonal code in standard basis. Hence, the maximal accumulated value in the SB accumulator is 1 and it can be stored in a 1-bit register. Therefore, in the SB decoding module, only one AND gate and an accumulator with one 1-bit register are used, resulting in less logical resources. An example of the decoding process is illustrated in Fig. 5. In Fig. 5(a), at the WB decoder of receiver 1, the accumulated value 3 in the positive part is larger than the accumulated value 1 in the negative part. By the WB decoding scheme, the decoded data is 1, which is equal to the source data bit from sender 1. In Fig. 5(b), at the SB decoder of receiver 1, the output value of the accumulator is 1, which is also equal to the source data bit from sender 1. Note that the

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decoding results in receiver 2 are also correct, but are not shown in the figure. Hence, both methods can reconstruct the original data bit from the sum signal by using their respective spreading codes.

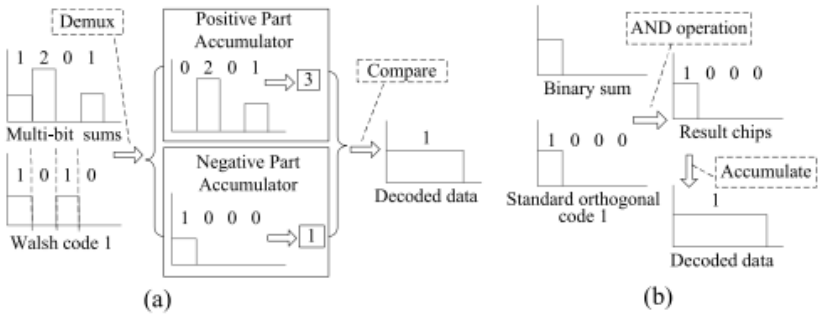

Fig. 5. Data decoding example. (a) WB decoding at receiver 1. (b) SB decoding at receiver 1.

4. RESULTS

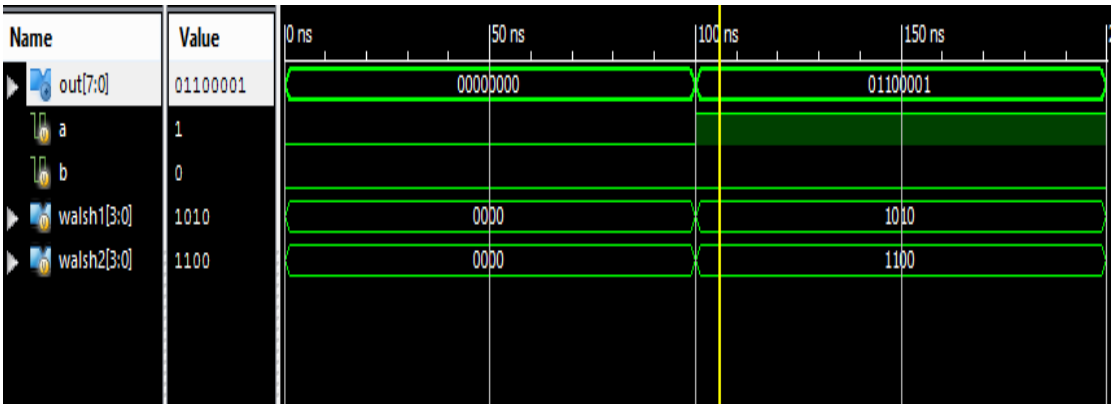

Fig.6. **wb encoder**

From fig.6 and fig.7 The encoded data from two senders are mixed together through xor operation, and a binary sum signal is generated.Therefore, the output signal is always a sequence of binary signal transferred to destination using one single wire. The progression of both the encoding schemes are depicted from fig.1. and fig.2. In WB decoding schemethe chip value of walsh code, the received multi bit sums are accumulated positive part or negative part by using comparator we have to compare positive and negative parts,if positive is greater than negative then the original data is 1, otherwise the original data is 0.

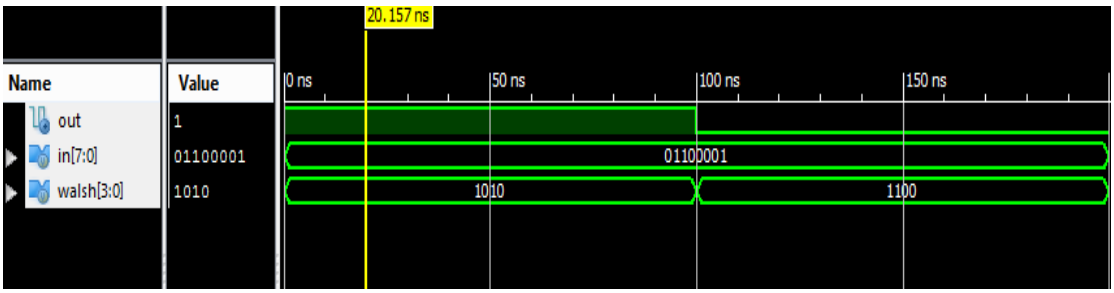

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Fig.7.**wb decoder**

From fig.8 and fig.9 in SB encoding scheme original data bit from a sender is fed into an AND gate in chip by chip manner and encoded data from a different senders are mixed together by an xor operation and a binary sum signal is generated. In sb decoding scheam the binary sum signal arrives at recevers,an AND operation is taken between binary sum and corresponding sum then the result is send to an accumulator the output of the accumulator will be the corresponding original data.

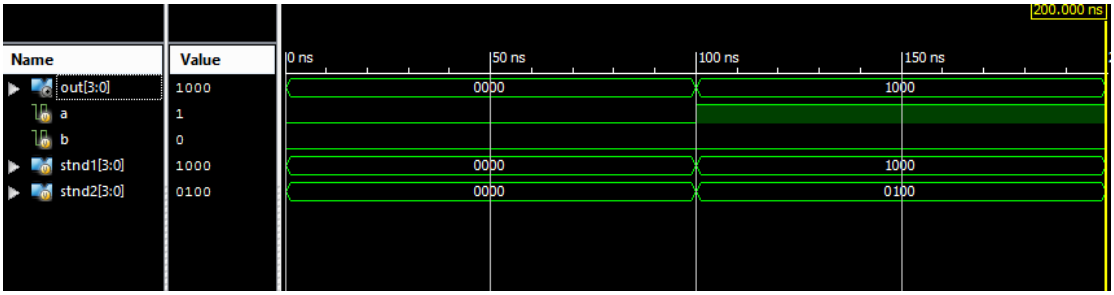

Fig.8. **sb encoder**

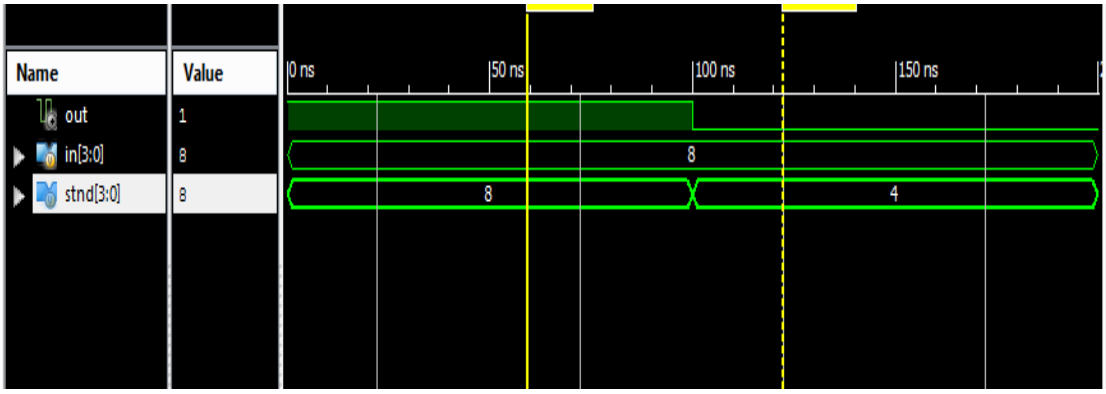

fig.9. **Sbdecoder**

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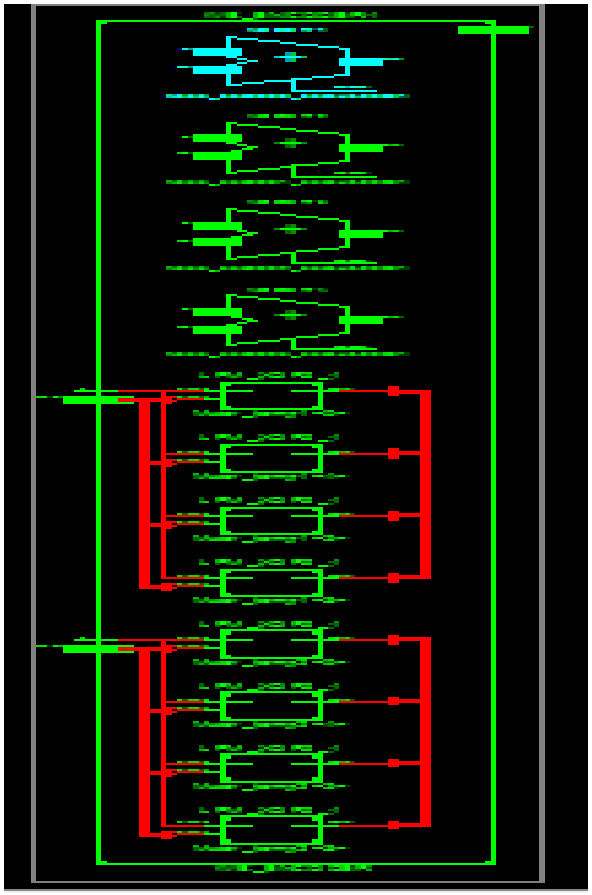

Rtlschrmatic

Design summary

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	4	5888	0%
Number of 4 input LUTs	8	11776	0%
Number of bonded IOBs	18	372	4%

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```
Timing constraint: Default path analysis
  Total number of paths / destination ports: 32 / 8
--------------------------------------------------------------------------------
Delay:               7.337ns (Levels of Logic = 3)
  Source:            b (PAD)
  Destination:       out<6> (PAD)

  Data Path: b to out<6>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             8   0.849   0.900  b_IBUF (b_IBUF)
     LUT4:I0->O            1   0.648   0.420  out<6>1 (out_6_OBUF)
     OBUF:I->O                 4.520          out_6_OBUF (out<6>)
    ----------------------------------------
    Total                      7.337ns (6.017ns logic, 1.320ns route)
                                       (82.0% logic, 18.0% route)
```

APPLICATIONS AND ADVANTAGES

- It contains larger capacity
- Gsm band width =200khz
- Easy to addition more users
- Better transmission data compare to tdma/fdma

5. CONCLUSION

In this paper, we introduced the concept of overloaded CDMA crossbars as the physical layer enabler of NoC routers. In overloaded CDMA, the communication channel is overloaded with nonorthogonal codes to increase the channel capacity. Two crossbar architectures that leverage the overloaded CDMA concept, namely, T-OCI and P-OCI, are advanced to increase the CDMA crossbar capacity by 100% and 2*N*× 100%, respectively, where *N* is the spreading code length. We exploited featured properties of the Walsh spread-ing code family employed in the classical CDMA crossbar to increase the number of router ports sharing the crossbar without altering the simple accumulator decoder architecture of the conventional CDMA crossbar. Generation procedures of nonorthogonal spreading codes are presented along with the reference and pipelined architectures for each crossbar variant. The T-/P-OCI crossbars were implemented. The performance of the OCI crossbars is compared with that of the conventional CDMA crossbar. The dynamic power is reduced by 45% for the T-OCI crossbar but increased by 133% for the P-OCI crossbar. The T-OCI crossbar utilizes 31% fewer resources, while the P-OCI crossbar uses 400% more resources compared with the conventional CDMA crossbar. The OCI crossbar suitability for NoCs has been established by analytically and experimentally evaluating a fully working OCI-based NoC. A 65-node OCI-based star NoC was realized and compared with an SDMA-based torus NoC generated by CONNECT. The evaluation results demonstrate the superiority of the OCI-based NoCs in terms of area and throughput.

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