International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

Development of N-Bit Adders and Subtractors with Reversible Logic Paradigm

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ABSTRACT

This work introduces a pioneering advancement in the development of N-Bit Reversible Adders and Subtractors (RAS) within the realm of digital circuit design, aimed at addressing the increasing demand for energy-efficient and environmentally conscious computing solutions. The conventional N-Bit adders, while known for their speed advantages, are plagued by inherent power dissipation and energy loss issues associated with irreversible computations. Recognizing this challenge, our proposed system strategically integrates reversible logic gates into the RAS architecture, offering a transformative solution to mitigate power consumption drawbacks while preserving computational speed.The paper begins with an overview of the significance of reversible computing in the context of modern digital systems, underscoring the crucial need for efficient adder designs in today's energy-conscious landscape. Subsequently, the limitations of conventional N-Bit adders are discussed, emphasizing their speed advantages but highlighting the sustainability concerns arising from power dissipation issues.The core of our contribution lies in the detailed exposition of the integration of reversible logic gates into the N-Bit RAS architecture. This innovative approach not only preserves the computational speed inherent to conventional adders but also substantially reduces power consumption, paving the way for a more sustainable and environmentally friendly design. The proposed system is validated through rigorous simulation and comparative analysis, demonstrating its efficacy and presenting a promising avenue for the advancement of energy-efficient digital circuits.

Keywords: reversible logic paradigm,N-Bit adders and subtractors,ras architecture.

1. INTRODUCTION

Advancements in VLSI have been done on three variables: area and Delay, power. Area improvement implies decreasing the space of rationale which possess on the pass on. This is done in both front-end and back-finish of structure. In front-end structure, legitimate portrayal of rearranged Boolean articulation and expelling unused states will prompt limit the door/transistor utilization. Segment, Floor arranging, Placement, and directing are act in back-finish of the plan which is finished by CAD tool[1].The CAD instrument have a particular calculation for each procedure to create a zone proficient structure like Power advancement. Force streamlining is to lessen the force dissemination of the plan which endures by working voltage, working recurrence, and exchanging movement. The initial two components are simply indicated in plan imperatives however exchanging action is a parameter which fluctuates powerfully, in light of the way which designs the rationale and information vectors. Delay improvement alludes to meeting the client imperatives in effective way with no infringement in any case, improving execution of the structure. Reversible Logic (RL) is an alluring rising innovation reasonable for the improvement of

ultra thick low-power superior advanced designs. RL which utilizes exhibit of coupled quantum dabs to execute Boolean rationale work. The benefit of RL lies in the incredibly high pressing densities conceivable because of the little size of the dabs, the rearranged interconnection, and the very low force defer item. An essential RL cells comprises of four quantum specks in a square cluster coupled by burrow hindrances. Electrons can burrow between the specks, yet can't leave the cells. On the off chance that two overabundance electrons are set in the cells, Coulomb shock will drive the electrons to dabs on inverse corners. There are in this manner two enthusiastically proportionate ground state polarizations can be marked rationale "0"and "1".The fundamental structure squares of the RL design are AND,OR and NOT. By utilizing the Majority boolean operation we can diminish the measure of deferral i.e by figuring the proliferation and generational conveys. Quantum specks are semiconductors kept in every one of the three elements of room or on the other hand, it very well may be noticed that Quantum dab is a basic charge compartment and it is three dimensionally restricted. The promising option of CMOS worldview is the RL which is utilized to speak to the data in parallel M' and twofold 'O' as far as electronic charge setup. In 1993, C. S. Loaned et al. first presented the hypothetical Quantum spot RL [2] and in mid 1999, C. S. Loaned et al. depicted the exploratory way to deal with structure RL cells with GaAs [3]. The dynamic conduct of RL was talked about with the assistance of the hart tree estimation; Quantum mechanics is likewise engaged with discovering the phone size and spot span of a solitary RL cells. Henceforth, RL became look into enthusiasm to set up as solid CMOS elective. During decades ago, in nanotechnology time, a thorough research has been completed in this space. RL is still in early stages stage, needs bunches of study for RL rationale design structure. The low force reversible rationale design configuration, tile based rationale design configuration just as its imperfection examination are prime issue space. The ternary figuring with RL is most testing task in this area since no such improvement is taken note. The multivalve figuring, explicitly ternary processing is a rising space of research due the potential preferences like more prominent information stockpiling capacity, quicker math tasks, better help for numerical examination, utilization of non-deterministic and heuristic approaches, correspondence convention and compelling answer for non-paired issues. Nano-scale rationale design developer is languishing from abandons that may happen during developer.

2. LITERATURE SURVEY

The development of electronic IT and interchanges has been mostly conceivable by nonstop advancement in silicon-based CMOS innovation. This ceaseless advancement has been kept up for the most part by its dimensional scaling, which brings about exponential development in both design thickness and execution. The decrease in cost perfunction has consistently been expanding the financial efficiency with each new innovation. Notwithstanding its versatility, the extraordinary design properties, for example, high information opposition, self - confinement, zero static force scattering, straightforward design and procedure steps have made CMOS transistors as the primary segments of CMOS ICs. Nonetheless, the components of CMOS transistor psychologists and approaches towards the nearness among source and channel, which decreases the capacity of the boolean operation terminal to control the potential dissemination and the progression of current in the channel district.In this way evading further decrease size.Dimensional scaling of CMOS transistors is arriving at their key physical cutoff points. Subsequently, look into has been effectively completed to locate an elective approach to keep on observing Moore's law. Among these endeavors, different sorts of elective memory and rationale designs, purported "Past CMOS Designs," have been proposed [35]. These nano-designs exploit the quantum mechanical marvels and ballistic vehicle qualities under lower flexibly voltage and thus low force

utilization. These designs are required to be utilized for ultra-high thickness incorporated electronic PCs because of their amazingly little size.

NWFETs have drawn promising consideration and have been viewed as a choice to proceed CMOS scaling, since their nonplanar geometry gives prevalent electrostatic control of the channel than the ordinary partners. The expanding consideration in Nano-wire investiboolean operation comes from a few key factors; their practical "base up" creation and high return reproducible electronic properties [36], which clear path for some developer difficulties, higher transporter portability, smooth surfaces and the capacity to deliver spiral and pivotal Nano-wire hetero-designs [37], better adaptability coming about because of the way that distance across of Nano-wires can be controlled down to well underneath 10 nm [38]. In any case, because of their littler measurements, the reversal charge changes from surface reversal to mass reversal because of quantum restriction. In this manner, varieties in Nano-wire measurements because of creation flaws can prompt annoyances in the bearer potential and dispersing that debase the charge transport attributes. Likewise, varieties in Nano-wire measurements may prompt a variety in FET edge voltage. Diminishing fluctuation is in this manner a key test in making Nano-wire FETs a practical innovation. Moreover, quantum control impacts make displaying of Nano-wire transistors a mind boggling issue. The material science identified with the activity of Nano-wire transistors should be all around enunciated so straightforward decreased models, including ballistic vehicle and sensible sub band parameters, can be produced for design configuration utilizing SPICE-like test systems [39].

Because of their one of kind material properties, CNTs have gotten overall consideration from many research works. CNTs are grapheme (which is a two-dimensional honeycomb cross section of carbon molecules) sheets folded up into chambers. They show either metallic or semiconducting properties relying upon the course how CNTs are moved up (amusingness). Since the band hole of semiconducting CNTs is conversely relative to their breadths, edge voltage can be effortlessly controlled [41].With their boss material properties, for example, the amazing mechanical and warm strength, huge current conveying limit, and high warm conductivity, the metallic nano-tubes are alluring as future interconnects [42]. Alongside these properties, the semiconducting nano tubes additionally show extraordinary focal points as a channel material of superior FETs. SETs [43] are extremely alluring designs for future enormous scope combination, because of their little size and low-power dissemination at great speed. The fundamental structure of SET comprises of three-terminals: channel, boolean operation, source, and the subsequent door, is a discretionary. A schematic of SET is practically equivalent to that of ordinary MOSFETs. Nonetheless, SET has a small conductive island coupled to a door anode with boolean operation capacitance. Source and channel cathodes are associated with the island through a passage hindrance (intersection). In SETs little voltage is applied between the sources and channel anodes by approaches for the "Coulomb barricade" marvel. New applications and models that misuse the remarkable usefulness of room temperature working SET designs have been grown, particularly by solid incorporation of SETs with FET designs to supplement the traditional Si CMOS execution. Deleboolean operation models incorporate SET/CMOS crossover multi-esteem rationale designs [44], multiband separating designs [45], simple example coordinating designs [46], affiliated acknowledgment undertakings [47], and others [48], in which trademark Coulomb bar motions of SETs are commonly used to lessen the quantity of designs. Note that specific parts of the design execution, particularly the room temperature activity; as of now surpass the hypothetical assessment of the rationale door parameters for 2-nm SETs. These designs have hypothetically evaluated most extreme activity temperature T~20 K, coordination thickness n~1011 cm-2, and speed of the request for 1 GHz [49]. Nonetheless, enormous

limit voltage variety keeps on blocking the acknowledgment of huge scope SET designs, making it hard for SETs to contend straightforwardly with CMOS designs used to actualize Boolean rationale activities.Designing forward leaps are expected to dispose of the size and foundation charge vacillations so as to stifle the edge voltage varieties. Single-electron draws near, speaking to a piece by a Single-electron ("bit state rationale") and the utilization of a solitary electron as a wellspring of irregular number ages, have been restricted to research center shows. The issue of the restricted fan-out, which is brought about by utilizing just a solitary electron in the really Single-electron designs, might be tackled by creative design plans, for example, the paired choice chart. Consequently, the lacks of CMOS have prompted noteworthy endeavors to discover proper other options and among the proposed arrangements; nano-scale advances, for example, Tunneling Phase Logic (TPL), Single Electron Tunneling (SET) and Quantum-dab RL (RL) have gotten extensive consideration [50]. Loathe looks into have proposed Quantum-spot potential executions for RL cell. As such Quantum-spot cell has introduced in [51]. An adiabatic exchanging worldview is created for clock-controlled pipelined RL designs. The double data is put away as electronic charge prompting less registering. Different examiners have been broadening the hypothetical examination of RL clusters. Vankamamidi et al. [52] have proposed elective approaches of amassing RL cell into helpful designs. They have created refined limited component models for door drained Quantum-dabs in semiconductors that can relate Dot inhabitance to specific predisposition conditions. They have introduced a basic timed atomic RL cells. The particles show natural bistability because of dipole charge arrangement, which unequivocally couples to its neighboring atoms. The investigation is basic, characteristic just of the chance of utilizing sub-atomic RL. Survey of the chance of executing RL in sub-atomic scale or in nano-magnets has been done . A lot of atomic designs for RL have been proposed, and one such 2-Dot RL has been actualized.

3. PROPOSED METHOD

3.1. INTRODUCTION:

The digital computer performs operations that seem to discard data in computer's history. In this, the machine state will be ambiguous [1]. The operations of computers incorporated to overwrite/erase the data and also consists a section which addresses a bit of data addressed at distinctive transfer instructions. Hence, the system is logically irreversible - its transition work lacks a single-esteemed inverse [2]. In development of nanotechnology, which is speed enhanced, less sized, and composed of highly convoluted engineering design than existing systems. The improvement in the technology has introduced a system considering the parameters like power and heat dissipation and clock frequency [3]. The highly enhancement in the clock frequency to get the better speed and increase the total transistors stuffed in a chip to accomplish required system results more power consumption. Almost in all the total logic gates for logical operations in old computer are irreversible. Hence, in every time a logical operation is performed to know input lost and it is dissipated as heat. For any digital design, the power loss must be considered for desired parameter [4]. The current technology improvement in the computer design are increased and also the power utilization also optimized by using the Reversible logic (RL). As per literature [5] with exponential development of heat produced because of information loss is major issue. The heat dissipation causes the reduction in the circuit’s execution time and lifetime. Thus, the use of reversibility can give low power consumption and heat dissipation system. In the work of literature [6] indicated how the reversibility can be achieved with zero power dissipation. Also, reversibility cannot cause information loss as like in irreversible. For reversibility circuit design we need set of reversible gates (RGs) and these kind of gates are available since last decades. As per literature [7] focused on

logical irreversibility which causes more heat losses. Accordingly, a computer must dissipate entropy (kTln 2) of energy for each data loss. An irreversible computer can made reversible by conserving the information. The reversible machine additional unit is used to store the every operation performed. In this machines the controls both the input and output information. Thus, as discussed in [7], this will prevent the information loss as it can be reused. Thus reversible computer halts the information, can be erased in middle results, the output can be reused as input. The research starts with the concept of reversibility [7] where at the ending of computation and first inverse of the transition work, the system can perform reverse computation. The Reversible circuit (RC) can create output from every input, i.e., there is a coordinated corresponding to input and output vectors. Thus, in a RC outputs will be equal to inputs. Basically, for an RC Conventional NOT gates is used. For designing the RC with the assistance of RG, some points to be considered: In RC, the Fan-out cannot permit.

- In RC, Loops cannot permit
- In RL, one more element is considered, which is more imperative than the total gates utilized with specific garbage outputs.

The un-utilized outputs from a RC/RG are called as "garbage". The RL imposes many design constraints that should be either ensured or optimized for actualizing a specific Boolean function.

- In RL circuit the inputs and outputs must be equal.
- In every input design, must have unique output design.
- Each output need to be will be used just once, i.e., fan out is not permit
- The RC must be non-cyclic computation that too in reversible manner for a system can be performed only if system comprises of RG.

A circuit can be “reversible”, when the input vector is uniquely recouped by output vector corresponding to input and output unit. The RL is a promising design paradigm offers efficient to design the computers with power dissipation. The RL can improve the standard of computing system. The reversible processing fundamentals are the relationship among entropy, heat transfer in a system. The RL guidelines the objective (reversible) device with equal lines of input and output delivering a processing domain.

The work of Yugandhar, K., et al [8] gives a new design method for array multiplier which uses more garbage outputs. Authors considered the 4-bit reversible high performance array multiplier (RHPAM) with reversible high performance adder (RHPA) synthesizing by utilizing the advanced bi-directional synthesis mechanism. Hence, for multiplier synthesis, the optimization of input bits and also the delay are not yet addressed except in the recent works which discusses about the post synthesis mechanism to reduce the quantum bits in the reversible multiplier.

Kamaraj, A., and P. Marichamy [9] introduced the fault tolerant ALU (FTALU) with no input carry with one ancillary input bit. Authors have examined new QR carry adder designs with no ancillary input bit gives improved delay. The reversible ALU in the existing literature is evaluated by garbage outputs, total RL used, QC and delay.

Amirthalakshmi, T. M., and S. Selvakumar Raja [10] have described concepts of 8-bit Reversible ALU (Proposed RAS). Also, designed and implemented high cost, efficient, fault tolerant, reversible ALU. In this more garbage outputs were compensated with fewer operations. The author concluded that the ALU performs all the logical operations better than existing methods not arithmetic operations.

Dasharatha, M., et al [11] addressed a concept that a function can be reversible if every vector produces equal number of outputs. In this the High speed ALU (HSALU) design is presented by making use of control signals and vedic multiplier units. With this design author has found that the proposed design is more effective as per garbage outputs and constant inputs are considered.

Rahim, B. Abdul, et al. [12] described a novel nonprogrammable logic gate and verified its implementation in ALU design using reversible multipliers. With this work author has found that the delay and are of ALU using RG should be low.

A new RL reversible based design technique is suggested by Oskouei, Saeed Mirzajani, and Ali Ghaffari [13] focused on the design for 8 bit reversible RL ALU and was utilized Xilinx as Synthesis tool. The ALU performs the reversible RL addition(RRLA), but it consumes more area and delay . Through this author achieved high propagation delay and high power dissipation by implementing 8bit arithmetical operations.

Shukla, Vandana, et al [14] described a design and implementation of reversible ALU of N-bit through low power addition (LPA). The ALU reduces the propagation delay and the power dissipation also reduced through clock gating but cost ineffective.

Table 1 summarizes the existing methods problems addressed and its outcome.

Table 1: Summary of Literature survey

Authors	Problem addressed	Outcome
Yugandhar, K[8]	Synthesis of reversible gates, Adder and multiplier design issues	ALU design with Low QC, delay and garbage output
Kamaraj, A., and P. Marichamy [9]	RL design Reduced minimum outputs	Reduced minimum outputs
Amirthalakshmi, T. M., and S. Selvakumar Raja [10]	Reversible design with sequential circuits	Better design than traditional RL design
Dasharatha, M., et al [11]	Adder design	ALU design with Low QC, delay, garbage output
Rahim, B. Abdul, et al. [12]	Design aspects of ALU using RL	Efficient ALU design for all mathematic operations
Oskouei, Saeed Mirzajani, and Ali Ghaffari [13]	Issues of ALU design process	Fault tolerant ALU
Shukla, Vandana, et al [14]	Off-chip biasing issues	Low power Nbit ALU design

To solve these problems, the paper is contributed as follows

- A novel full adder is designed with fredkin gate and Feynman gate combinations; this reduces the delay and area requirement.
- An N-bit reversible RCA has developed utilizing the reversible full adder.

- An N-bit reversible array multiplier has been developed by utilizing the fredkin gates and N-bit reversible RCA.
- An N-bit Reversible adder subtractor was designed; using this adder subtractor and array multiplier an N-bit Reversible ALU was developed.
- A detailed analysis of results has been presented with comparison to the existing method .the results shows that proposed method is area, power and delay efficient.

Rest of the paper as follows: section 2 gives the detailed analysis over reversible logic gates with its unique properties also introduces operations of Feynman gate and Fredkin gate. Section 3 gives the detailed analysis of reversible designs such as proposed Full adder, proposed N-bit RCA, proposed N-bit array multiplier, proposed N-bit adder subtractor and N-bit ALU. Section 4 gives the detailed analysis on results with respect to both simulation and synthesis outcome and comparative analysis also performed with various convention approaches. Section 5 deals about conclusion and future works of proposed methods.

3.2. REVERSIBLE LOGIC GATES

Reversible logic gates are developed with the pass transistor technology using quantum dot cellular automata. The reversible logic gates are preferable to design the chips because they exhibit the following properties.

PROPERTIES OF REVERSIBLE LOGIC GATES

PROPERTY 1: BIDIRECTIONAL PROPERTY

Using this property in chip level implementation so both input and output pins are interchangeable. In fig 1, if A, B are the inputs of Feynman gate, then R, S are acts as output pins. Due to the quantum data reversible nature, if the inputs are applied at the outputs side, then R, S acts as input pins and A, B acts as outputs correspondingly.

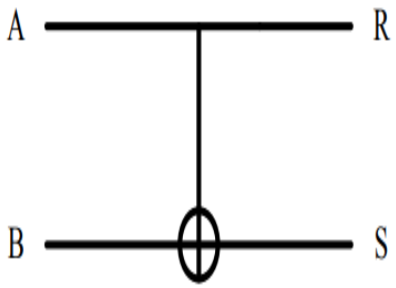

Fig 1: Bidirectional property of Feynman Gate

In case of basic gates, they wont supports this property maintains the unidirectional data transfer. Normally, ICs consists of multiple numbers of gates. Thus, by the use of bidirectional property , the path delay will be reduced as both inputs and outputs can be interchangeable and logic optimization also achieved .

PROPERTY 2: FAN-IN FAN-OUT CAPACITY

Every reversible logic gate supports fan-in and fan-out property because the number of input pins and number of output pins will remain same. So, the load on the chip will be reduces effectively even number of inputs and outputs are mismatch. In case of basic gates, they consist of multiple numbers of input pins

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and only one output pin. So, to perform the any output operation using multiple inputs creates the fan-out problem in the basic gates.

PROPERTY 3: NUMBER OF OPERATIONS

The reversible logic gates supports N-number of logical operations based on the number of input-output pins .for example, Feynman gate acts as both buffer and ex-or operation. In case of basic gates they dedicated to only one operation.

PROPERTY 4: QUANTUM COST

The quantum cost required for the reversible logic gate is very less compared to the basic gates.

FEYNMAN GATE

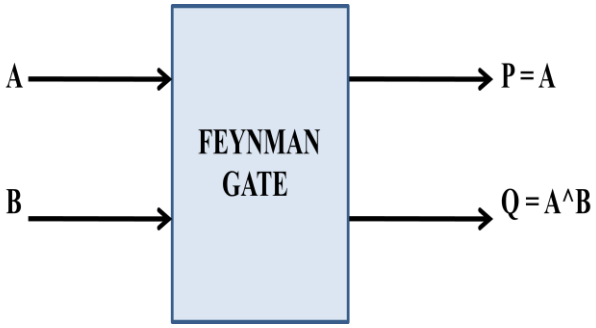

Fig 2: operation of Feynman Gate

Figure 2 gives the detailed operation of Feynman gate, it acts as both buffer and exclusive or gate.

FREDKIN GATE

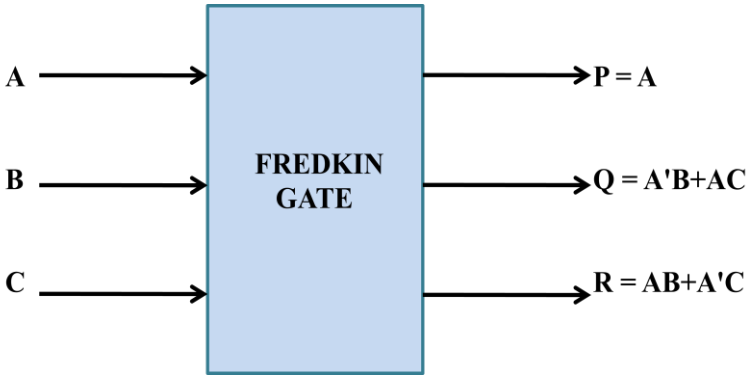

Fig 3: operation of Fredkin Gate

Fredkin gate is a universal gate, any arithmetical and logical operation can be implemented very effectively with low area, delay and power consumption compared to basic gates. Thus it is effectively used in the ALU operation. The detailed structure of Fredkin Gate presented in Fig 3.

The main applications of Fredkin gate is that, it acts as AND gate as well as OR gate by controlling the input pins. If C input of Fredkin gate is 1'b0, then R output of Fredkin gate acts as AND operation.

$$C = 0 \rightarrow R = A\&B + \bar{A}\&1'b0 = A\&B \qquad (1)$$

If B input of Fredkin gate is 1'b1, then R output of Fredkin gate acts as OR operation respectively.

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$$B = 1 \rightarrow R = A\&(1'b1) + \bar{A}\&C = A + \bar{A}\&C = A + C \quad (2)$$

PERES GATE

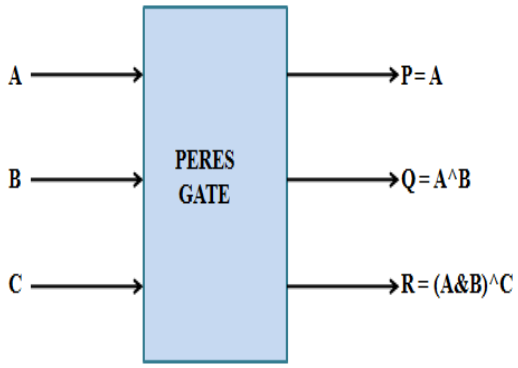

Figure 4 gives the detailed operation of Peres gate, it acts as both buffer and exclusive or gate. If the input C is zero, then the outputs R acts as AND function respectively.

3.3.PROPOSED REVERSIBLE FULL ADDER-SUBTRACTOR

The design of Reversible full adder and subtractor (RFAS) will be effectively used for the purpose of ALU by utilizing the single architecture for both operations.

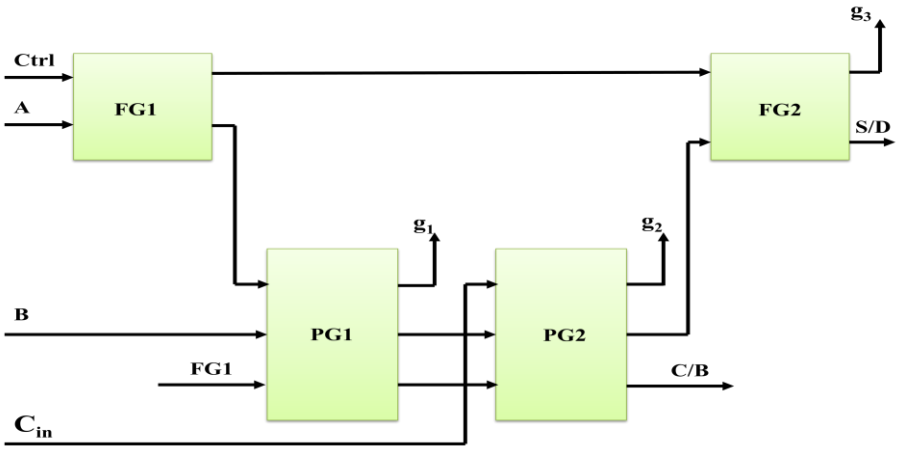

Fig 5: architecture of RFAS

From the figure 5, it is observed that if Ctrl input is zero, the design acts as reversible Full adder. if Ctrl input is one, the design acts as reversible Full subtractor. And subtraction operation developed based on the twos compliment addition.

$$Ctrl = 0 \rightarrow out = A + B = A + B + Ctrl$$

$$Ctrl = 1 \rightarrow out = A - B = A + \bar{B} + 1 = A + \bar{B} + Ctrl$$

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4. SIMULATION RESULTS

All the proposed designs have been programmed and designed using Xilinx ISE software this software tool provides the two categories of outputs named as simulation and synthesis. The simulation results give the detailed analysis of proposed design with respect to inputs, output byte level combinations. Through simulation analysis of accuracy of the addition, multiplication process estimated easily by applying the different combination inputs and by monitoring various outputs. Through the synthesis results the utilization of area with respect to the programmable logic blocks (PLBs), look up tables (LUT) will be achieved. And also time summary with respect to various path delays will be obtained and power summary generated using the static and dynamic power consumed.

4.1 CMOS ADDER-SUBTRACTOR OUTPUTS

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	2682	63400	4%
Number of fully used LUT-FF pairs	0	2682	0%
Number of bonded IOBs	132	210	62%

Figure 6 CMOS ADDER-SUBTRACTOR Design Summary

```
LUT4:I1->O            2    0.043   0.554  R3/[20].R2/aa[30].b1/f2/Mxor_q_xo<0>1
LUT6:I0->O            3    0.043   0.438  R3/[21].R2/aa[29].b1/u2/Mxor_r_xo<0>1
LUT4:I1->O            2    0.043   0.554  R3/[21].R2/aa[30].b1/f2/Mxor_q_xo<0>1
LUT6:I0->O            3    0.043   0.438  R3/[22].R2/aa[29].b1/u2/Mxor_r_xo<0>1
LUT4:I1->O            2    0.043   0.555  R3/[22].R2/aa[30].b1/f2/Mxor_q_xo<0>1
LUT6:I0->O            3    0.043   0.438  R3/[23].R2/aa[29].b1/u2/Mxor_r_xo<0>1
LUT4:I1->O            2    0.043   0.555  R3/[23].R2/aa[30].b1/f2/Mxor_q_xo<0>1
LUT6:I0->O            3    0.043   0.438  R3/[24].R2/aa[29].b1/u2/Mxor_r_xo<0>1
LUT4:I1->O            2    0.043   0.555  R3/[24].R2/aa[30].b1/f2/Mxor_q_xo<0>1
LUT6:I0->O            3    0.043   0.438  R3/[25].R2/aa[29].b1/u2/Mxor_r_xo<0>1
LUT4:I1->O            2    0.043   0.555  R3/[25].R2/aa[30].b1/f2/Mxor_q_xo<0>1
LUT6:I0->O            3    0.043   0.438  R3/[26].R2/aa[29].b1/u2/Mxor_r_xo<0>1
LUT4:I1->O            2    0.043   0.554  R3/[26].R2/aa[30].b1/f2/Mxor_q_xo<0>1
LUT6:I0->O            3    0.043   0.438  R3/[27].R2/aa[29].b1/u2/Mxor_r_xo<0>1
LUT4:I1->O            2    0.043   0.554  R3/[27].R2/aa[30].b1/f2/Mxor_q_xo<0>1
LUT6:I0->O            3    0.043   0.438  R3/[28].R2/aa[29].b1/u2/Mxor_r_xo<0>1
LUT4:I1->O            2    0.043   0.554  R3/[28].R2/aa[30].b1/f2/Mxor_q_xo<0>1
LUT6:I0->O            3    0.043   0.438  R3/[29].R2/aa[29].b1/u2/Mxor_r_xo<0>1
LUT6:I3->O            1    0.043   0.289  Mmux_out321 (Mmux_out32)
LUT3:I2->O            1    0.043   0.279  Mmux_out322 (out_63_OBUF)
OBUF:I->O                  0.000          out_63_OBUF (out<63>)
----------------------------------------
Total                     39.557ns (3.311ns logic, 36.246ns route)
                                   (8.4% logic, 91.6% route)
```

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Figure 7 CMOS ADDER-SUBTRACTOR Time Summary

```
Macro Statistics
# Adders/Subtractors                                   : 60
 12-bit adder                                         : 40
 8-bit adder                                          : 20
# Multiplexers                                         : 1
 65-bit 8-to-1 multiplexer                            : 1
# Xors                                                 : 1947
 1-bit xor2                                           : 1897
 15-bit xor2                                          : 25
 16-bit xor2                                          : 25
```

Figure 8: CMOS ADDER-SUBTRACTOR XOR utilization

```
Primitive and Black Box Usage:
------------------------------
# BELS                                 : 3427
#      GND                             : 1
#      LUT2                            : 418
#      LUT3                            : 312
#      LUT4                            : 301
#      LUT5                            : 390
#      LUT6                            : 1261
#      MUXCY                           : 342
#      MUXF7                           : 34
#      XORCY                           : 368
# IO Buffers                           : 132
#      IBUF                            : 67
#      OBUF                            : 65
```

Figure 9 CMOS **ADDER-SUBTRACTOR** LUT utilization

4.2 Reversible RAS outcomes

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	2151	63400	3%
Number of fully used LUT-FF pairs	0	2151	0%
Number of bonded IOBs	131	210	62%

Figure 9: Proposed RAS Design Summary

Figure 8 represents the design summary; from this it is observed that the proposed Reversible ALU consumes the less area, less LUTs.

International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
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ISSN: 2457-0362

```
LUT5:I4->O            1   0.097   0.295  VV11/Kk2/K1/GC7/G3 (VV11/Kk2/K1/GC7/G2)
LUT6:I5->O            1   0.097   0.379  VV11/Kk2/K1/GC16/G4_SW0 (N201)
LUT6:I4->O            7   0.097   0.323  VV11/Kk2/K1/GC16/G4 (VV11/Kk2/cout1)
LUT5:I4->O            3   0.097   0.305  VV11/Kk2/K2/GC3/G1 (VV11/Kk2/K2/s<3>)
LUT5:I4->O            3   0.097   0.305  VV11/Kk2/K2/GC7/G1 (VV11/Kk2/K2/v<7>)
LUT5:I4->O            3   0.097   0.566  VV11/Kk2/K2/GC16/G1 (VV11/cout2)
LUT6:I2->O            5   0.097   0.575  VV11/Kk3/K1/GC1/G1 (VV11/Kk3/K1/q<1>)
LUT5:I1->O            2   0.097   0.516  VV11/Kk3/K1/GC3/G (VV11/Kk3/K1/s<3>)
LUT6:I3->O            2   0.097   0.299  VV11/Kk3/K1/GC7/G3_SW0 (N259)
LUT5:I4->O            1   0.097   0.295  VV11/Kk3/K1/GC7/G3 (VV11/Kk3/K1/GC7/G2)
LUT6:I5->O            1   0.097   0.379  VV11/Kk3/K1/GC16/G4_SW0 (N197)
LUT6:I4->O            4   0.097   0.309  VV11/Kk3/K1/GC16/G4 (VV11/Kk3/cout1)
LUT6:I5->O            4   0.097   0.570  VV11/Kk3/K2/GC1/G1 (VV11/Kk3/K2/q<1>)
LUT6:I2->O            2   0.097   0.688  VV11/Kk3/K2/GC6/G11 (VV11/Kk3/K2/GC6/G1)
LUT5:I0->O            3   0.097   0.521  VV11/Kk3/K2/GC8/G11 (VV11/Kk3/K2/GC8/G1)
LUT6:I3->O            2   0.097   0.688  VV11/Kk3/K2/GC10/G1 (VV11/Kk3/K2/v<10>)
LUT6:I1->O            1   0.097   0.295  VV11/Kk3/K2/GC14/G1 (VV11/Kk3/K2/v<14>)
LUT5:I4->O            1   0.097   0.279  Mmux_out331 (out_63_OBUF)
OBUF:I->O                 0.000          out_63_OBUF (out<63>)
----------------------------------------
Total                      26.859ns (5.710ns logic, 21.149ns route)
                                    (21.3% logic, 78.7% route)
```

Figure 10: Proposed RAS Time Summary

```
Advanced HDL Synthesis Report

Macro Statistics
# Multiplexers                                          : 1
 64-bit 8-to-1 multiplexer                             : 1
# Xors                                                  : 6337
 1-bit xor2                                            : 6336
 64-bit xor2                                           : 1
```

Figure 11 Proposed RAS XOR summary

```
Top Level Output File Name         : ALUNBIT.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 2182
#      LUT2                        : 508
#      LUT3                        : 43
#      LUT4                        : 469
#      LUT5                        : 154
#      LUT6                        : 977
#      MUXF7                       : 31
# IO Buffers                       : 131
#      IBUF                        : 67
#      OBUF                        : 64
```

Figure 12: Proposed RAS LUT summary

Figure 12 represents the time summary; from this it is observed that the proposed Reversible ALU consumes less time with less logical delay and route delay.

Table 1: Performance Comparison

Parameter	CMOS Adder-subtractor	Proposed RAS	%improved
LUTS	2682	2152	19.7614% decrease
Delay(ns)	**39.557**	26.859	32.1005% decrease
Adders/subtractors	**60**	0	NA
Xors	**1947**	6637	NA
BELS	**3427**	2182	36.3292% decrease
LUT2	**418**	508	21.5311% increase
LUT3	**312**	43	86.2179% decrease
LUT4	**301**	469	55.814% increase
LUT5	**390**	154	60.5128% decrease
LUT6	**1261**	977	22.5218% decrease
MUXF7	**34**	31	8.82353% decrease

From Table 2, it is concluded that the proposed RAS consumes the less area with respect to XORs, LUTs and it also consumes the less delay as compared to the conventional CMOS ALU respectively..

5. Conclusion and Future Scope

Conclusion:

In conclusion, this paper introduces a paradigm-shifting approach to N-Bit Reversible Adders and Subtractors (RAS) by integrating reversible logic gates, effectively mitigating the power dissipation issues inherent in conventional adders. The presented system not only maintains the computational speed advantages of traditional adders but also significantly reduces energy consumption, addressing the growing need for energy-efficient digital circuit designs. The simulation and comparative analysis affirm the effectiveness of the proposed N-Bit RAS with reversible logic gates, marking a substantial step towards sustainable and environmentally conscious computing solutions.

REFERENCES

[1]Zulehner, Alwin, and Robert Wille. "One-pass design of reversible circuits: Combining embedding and synthesis for reversible logic." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 37.5 (2017): 996-1008.

[2]Raveendran, Sithara, et al. "Design and Implementation of Reversible Logic based RGB to Gray scale Color Space Converter." *TENCON 2018-2018 IEEE Region 10 Conference*. IEEE, 2018.

[3]Qian, Junzhou, and Junchao Wang. "A 4-bit array multiplier design by reversible logic." *Information Technology*. CRC Press, 2015. 21-24.

[4]Ghosh, Arpita, and S. K. Sarkar. "Performance Investigation of Nanoscale Reversible Logic gates designed with SE-TLG Approach." *International Journal of Electronics* just-accepted (2020).

[5]Gaur, Hari Mohan, Ashutosh Kumar Singh, and Umesh Ghanekar. "In-depth comparative analysis of reversible gates for designing logic circuits." Procedia Computer Science 125 (2018): 810-817.

[6]Sasamal, Trailokya Nath, Ashutosh Kumar Singh, and Anand Mohan. "Reversible logic circuit synthesis and optimization using adaptive genetic algorithm." *Procedia Computer Science* 70 (2015): 407-413.

[7]Ahmad, Peer Zahoor, et al. "A novel reversible logic gate and its systematic approach to implement cost-efficient arithmetic logic circuits using QCA." *Data in brief* 15 (2017): 701-708.

[8].Yugandhar, K., et al. "High Performance Array Multiplier using Reversible Logic Structure." *2018 International Conference on Current Trends towards Converging Technologies (ICCTCT)*. IEEE, 2018.

[9]Kamaraj, A., and P. Marichamy. "Design of integrated reversible fault-tolerant arithmetic and logic unit." *Microprocessors and Microsystems* 69 (2019): 16-23.

[10]Amirthalakshmi, T. M., and S. Selvakumar Raja. "Design and analysis of low power 8-bit ALU on reversible logic for nanoprocessors." *Journal of Ambient Intelligence and Humanized Computing* (2018): 1-19.

[11]Dasharatha, M., et al. "VLSI Design and Synthesis of Reduced Power and High Speed ALU Using Reversible Gates and Vedic Multiplier." *Advances in Decision Sciences, Image Processing, Security and Computer Vision*. Springer, Cham, 2020. 272-280.

[12] Rahim, B. Abdul, et al. "Design of a Power Efficient ALU Using Reversible Logic Gates." International Conference on Communications and Cyber Physical Engineering 2018. Springer, Singapore, 2018.

[13]Oskouei, Saeed Mirzajani, and Ali Ghaffari. "Designing a new reversible ALU by QCA for reducing occupation area." *The Journal of Supercomputing* 75.8 (2019): 5118-5144.

[14]Shukla, Vandana, et al. "Reversible Realization of N-bit arithmetic circuit for low power loss ALU applications." *Procedia Computer Science* 125 (2018): 847-854.