International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

# DESIGN A HIGH PERFORMANCE MEMORY COMPUTING WITH DUAL ADDRESS SRAM ARCHITECTURE

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**ABSTRACT: In this paper design a high performance memory computing with dual address SRAM architecture is implemented. The main intent of this project is to reduce the delay and improve the performance of system. Initially input is tested unit BIST and transfers the data to SRAM control circuit block. If there are any errors in obtained data CRC will detect and correct it and gives the accurate data. Address control unit decodes address of data in two ways they are row decoder and column decoder. Row decoder decodes the data in row format and column decoder will decodes the data in column format. At last the row and column data will be saved in SRAM array memory. From this data will perform read and write operations. This is simulated using Xilinx technology. From simulation results it can observe that effective output is obtained in terms of delay and area.**

**KEY WORDS: Memory, Dual Address, SRAM (Static Random Access Memory), Row Decoder, Column Decoder, CRC (Cyclic Redundancy Check).**

## I. INTRODUCTION

Static Random Access Memory (SRAM) involves a huge segment of a framework on-a-chip (SoC) and has a remarkable commitment to the all out force utilization and region of the SoC. Since region is an Important factor when structuring circuits, memory configuration engineers mean to put however many cells as would be prudent per segment to permit sharing of fringe hardware [1].The regular 6T and 8T cells are incredibly restricted by their failure to work in longer segments. In most recent couple of years to achieve the superior CMOS gadget, scaling is utilized [1].

Low power circuit operation is a vital metric for the present incorporated circuits. As compact battery powered electronic devices like small radio devices, cell phones and convenient computers are winding up more mind amazed and common, the interest for expanded battery life requires to search out new innovations and circuit systems that give superior and long operational circumstances. In non-compact applications additionally, lessening power scattering is turning into an important basic issue [1]. Additionally, so as to meet the ongoing execution in computers is complex applications, it is important to have a base event moreover. However, as technology is invariably scaled, spilling currents turn into a noteworthy supporter of the separate power spreading.

A diminishment in power supply voltage is important to lessen dynamic power and stay away from unwavering quality issues in profound sub micron administrations [2]. Voltage scaling goes with supply voltage scaling to keep up the execution, yet it exponentially builds the sub threshold spilling currents. This lessened supply voltage and expanded spilling cause securely and untrustworthy operation of circuits. Thus, in this proposal, an active is made to outline digital CMOS circuits that have lessened dynamic and spilling power with a worthy deferral and noisy edge. Different power decrease methods are INTRODUCED and investigated for their application in three different digital CMOS circuits [3].

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The developing interest of compact battery worked frameworks has made strong skilled processors a need. For applications like suitable figuring active productivity takes top generally need. These inserted frameworks need continued charging of their batteries. The issue is gradually extreme in the remote sensor systems which are sent for checking the natural parameters [4].

Memory structures have become inseparable piece of current VLSI frameworks. Semiconductor memory is directly simply remain solitary memory chip as well as a vital piece of complex VLSI frameworks. The dominating model for streamlining is regularly to press in however much as memory as could reasonably be expected in a given region. This pattern toward compact figuring has prompted power issues in memory .The pattern of scaling of gadget sizes, low limit voltage, and ultra-slim gate oxide have progressively been tested by fluctuation, and along these lines, by dependability related issues.

SRAM's effect has gotten particularly significant because of the rise of battery fueled convenient gadgets and low force sensor applications. Most SRAM plan exertion has been directed to encourage voltage scaling and improving yield. The traditionally actualized six transistor (7T) cell in SRAMs permits high thickness, bit-interleaving and quick differential detecting however experiences half-select security, read-upset dependability, and clashing peruse and compose measuring. Past endeavors to unravel these issues have incorporated the usage of help methods, novel cell structure, engineering enhancements, or innovative turns of events Most SRAMs are developed using multi VDD biasing to achieve low power consumptions and low delays with the use of Voltage level shifters [5].

## II.EXISTED SYSTEM

In modern VLSI ICs the linear decoders are widely used the structure of such type of decoders is based on the following logic cells: inverters with number equal to numbers of decoder inputs, NAND and NOR logic cells with number equal to the number of outputs of decoder and predecoder cell designed with NAND and NOR logic cells. NAND and NOR cells are preferable because they contain 1.5 times smaller number of transistors compared to the AND and OR cells. Implemented researches shown that design of 2-4 decoder according to the above mention approaches requires 2 inverters for NAND or NOR logic gates hence totally 20 MOS transistors are necessary. The implementation of the 4-16 decoder will require 4 inverters, 8 pre decoders designed with NAND and NOR logic cells, 16 NAND or NOR output stages. So, the total number of transistors used in such type of design equals to 104.

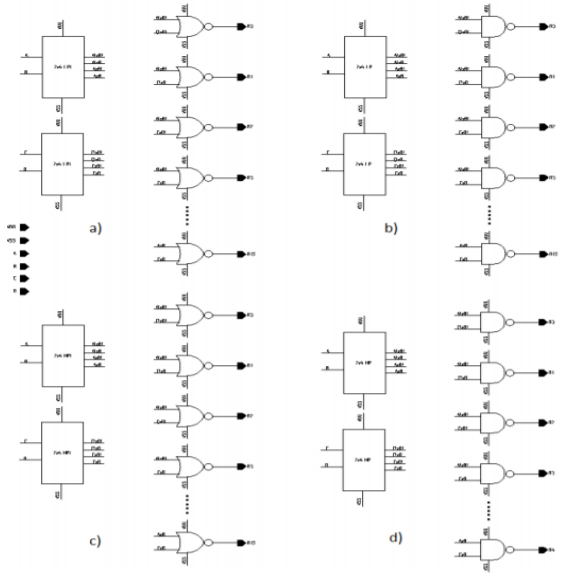


**Fig. 1: SCHEMATIC OF THE EXISTED SYSTEM**

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Expanding the memory size makes the necessary level of unwavering quality difficult to please. This makes the main test for the SRAMs in cutting edge innovation hubs. The force utilization increments with the progressed CMOS advances. CMOS scaling requires not just low edge voltages to hold the gadget exchanging speeds, yet in addition ultra-flimsy gate oxides to keep up the present drive and monitor limit voltage varieties when managing short-channel impacts. Low limit voltage brings about an exponential increment in the sub-edge spillage current which adds to the static force utilization. Charging/releasing enormous piece lines' capacitance speaks to a huge segment of intensity utilization during a compose or read tasks, which speaks to the dynamic force.

## III.PROPOSED SYSTEM

The below figure (2) shows the block diagram of proposed system. Initially input is tested unit BIST and transfers the data to SRAM control circuit block. If there are any errors in obtained data CRC will detect and correct it and gives the accurate data. Address control unit decodes address of data in two ways they are row decoder and column decoder. Row decoder decodes the data in row format and column decoder will decodes the data in column format. At last the row and column data will be saved in SRAM array memory. From this data will perform read and write operations.

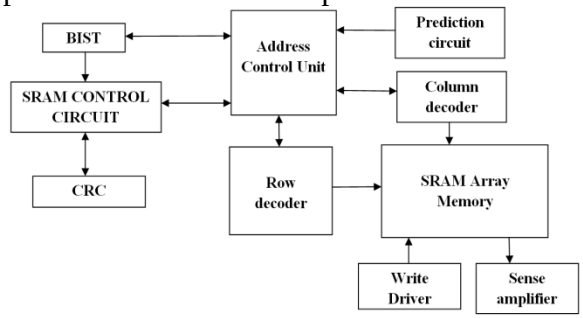


**Fig. 2: BLOCK DIAGRAM OF PROPOSED SYSTEM**

### 1. SRAM

With the fast development in the semiconductor business, the pressing thickness of incorporated circuits ICs is ever expanding and the segment or transistor size is lessening. Static Random-access memory (SRAM) is an indispensable piece of cutting edge electronic gadgets. To accomplish higher coordination thickness of SRAM, a base estimated memory cell is alluring, however this essentially expands spillage current. In lower innovation, backup spillage is a central point adding to add up to spillage current. Versatile handheld gadgets likewise stay in reserve mode for extensive measures of time; thus, spillage in this mode additionally is a genuine worry as it decreases the battery reinforcement time. To decrease the spillage current in Complex Metal Oxide Semiconductor (CMOS) innovation, the circuit is worked on lower flexibly voltage yet this thusly hinders the speed of the circuit.

Postponement can be diminished by utilizing transistors with a lower limit voltage; however this again builds the spillage current (fundamentally the sub-edge spillage current). There are differentiating prerequisites and great advancement is important to structure a memory cell with lower backup spillage and great solidness. Lower voltages and littler size reason critical corruption of information steadiness in cells. The soundness of SRAM relies upon the static, which thus relies upon different other cell boundaries.

### 2. CYCLIC REDUNDANCY CHECK

The main intent of cyclic redundancy check is to detect the errors and correct the errors.

### 3. ROW ADDRESS

These are the set of cells that generate the word line signals from the word decoders.

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This structure takes a set of n address lines and generates word lines. At most, one of the word lines is active at a time.

## 4. COLUMN ADDRESS

Column address select particular bit lines for being connected to sense amplifiers. This is accomplished either by sensing every bit line and getting a few of them out or by using pass gates to enable them to a few sense amplifier inputs

## IV. RESULTS

The below figure (3) shows the RTL Schematic of proposed system.

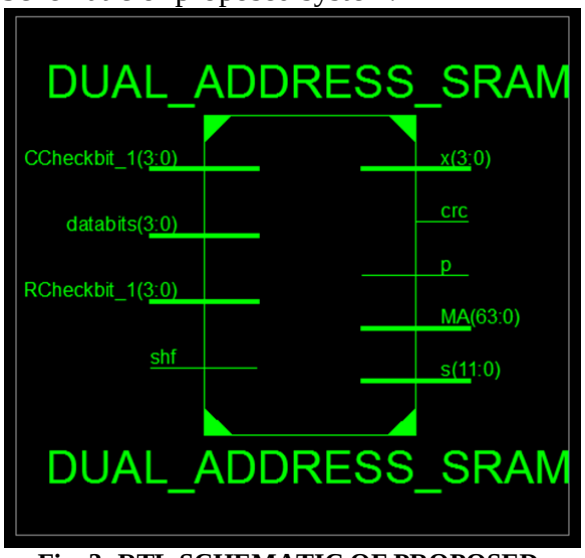


**Fig. 3: RTL SCHEMATIC OF PROPOSED SYSTEM**

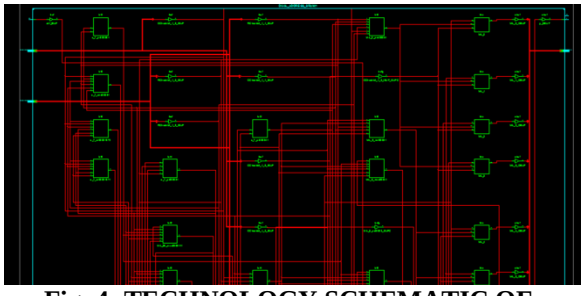

**Fig. 4: TECHNOLOGY SCHEMATIC OF PROPOSED SYSTEM**

The below figure (5) shows the output waveform of proposed system.

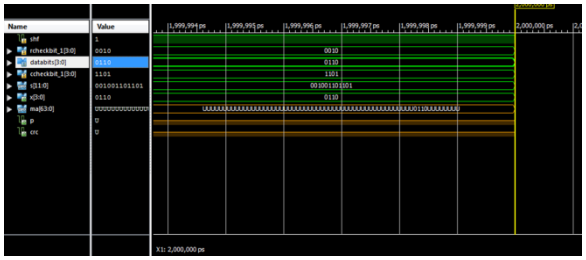

**Fig. 5: OUTPUT WAVEFORM OF PROPOSED SYSTEM**

## V.CONCLUSION

Hence in this paper design a high performance memory computing with dual address SRAM architecture is implemented. Address control unit decodes address of data in two ways they are row decoder and column decoder. From this data will perform read and write operations. This is simulated using Xilinx technology. From simulation results it can observe that effective output is obtained in terms of delay and area.

## VI.REFERENCES

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