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A MODIFIED FULL ADDER (MFA) BASED MULTIPLIER DESIGN FOR LOW POWER VLSI CIRCUIT APPLICATIONS

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ABSTRACT

Designing multipliers that are of high-speed, low power, and regular in layout are of substantial research interest. Speed of the multiplier can be increased by reducing the generated partial products. Many attempts have been made to reduce the number of partial products generated in a multiplication process one of them is array multiplier. array multiplier half adder have been used to sum the carry products in reduced time. Achieving high speed integrated circuits with low power consumption is a major concern for the VLSI circuit designers. Most arithmetic operations are done using multiplier, which is the major power consuming element in the digital circuits. Basically the process of multiplication is realized in hardware in terms of shift and add operation. The optimization of adder has led to the improvement in performance of multiplier. In this paper, a modified full adder using multiplexer is proposed to achieve low power consumption of multiplier. To analyze the efficiency of proposed design, the conventional array multiplier structure is used. The designs are developed using Verilog HDL and the functionalities are verified through simulation using Xilinx.

INTRODUCTION

The power consumption, delay and area are always been an important design considerations for any chip designer. Many DSP structures incorporate multipliers in their design. Delay of the circuit inevitably changes with the delay of the multiplier. Therefore research is going on to reduce the delay of multiplier so that the delay of whole circuit can be reduced. An early description of the array multiplier was given by [1]. array multiplier has been evolved as high speed and area efficient multiplier. The array multiplier involves ANDing of multiplier and multiplicand bits for the generation of partial products. In second phase full adders and half adders has been used for the reduction of generated partial products in two rows. Followed by addition of two rows using fast carry adders in the third stage.

In recent years a lot of research work has been carried out [2], [3], [4], [9], [10] to reduce the complexity of the multiplier. In [2], a novel method is used for reduction of complexity of array multiplier in terms of number of half adders. In [3], further improvement to the method introduced in [2] is carried out by incorporating one more half adder to the right most columns, results in a drastic area reduction. In addition to that, in [4] Booth encoding approach along with compressor has been used to reduce the area as well as latency. Furthermore, in [5] the conventional half adder and full adder in

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the second stage are replaced with XOR-XNOR based 3:2, 4:2 and 5:2 compressors which brings an increase in speed of operation. An efficient approach is proposed by estimating the power of each stage of the reduction tree using probabilistic gate-level power estimator [6].

Due to that the switching power is reduced by optimizing the transitions activity in the partial product tree. In [7], the reordering of partial products is employed in such a way so as to reduce the switching activity which leads to reduction in power. Partitioning the partial product tree into four groups and applying Dadda to one group and array multiplier to another and so on also achieves power reduction [8]. In [9], a modified full adder using 4:1 multiplexers is used in the reduction phase to reduce the power. In [11], full adder is designed using six 2:1 multiplexers. The architecture is designed in a unique way, such that it is reducing the short circuit current as well as the transition activity, thus the power is also getting reduced. But the area is increasing significantly. This work mainly deals with the replacement of full adders with modified full adder in the reduction phase of the array multiplier. In the proposed method, a modified full adder using multiplexer is applied to achieve power reduction compared to the existing techniques with a small area and delay improvement .

Gone are the days when huge computers made of vacuum tubes sat humming in entire dedicated rooms and could do about 360 multiplications of 10 digit numbers in a second. Though they were heralded as the fastest computing machines of that time, they surely don't stand a chance when compared to the modern day machines. Modern day computers are getting smaller, faster, and cheaper and more power efficient every progressing second. But what drove this change? The whole domain of computing ushered into a new dawn of electronic miniaturization with the advent of semiconductor transistor by Bardeen (1947-48) and then the Bipolar Transistor by Shockley (1949) in the Bell Laboratory.

LITERATURE SURVEY

[1] Vojin G. Oklobdzija, David Villeger, Simon S. Liu, "Method for Speed Optimized Partial Product Reduction and Generation of Fast Parallel Multipliers Using an Algorithmic Approach," (vol. 45, No.3) pp. 294-306, March 1996.

This literature describes about, a method and an algorithm for generation of a parallel multiplier, which is optimized for speed. This method is applicable to any multiplier size and adaptable to any technology for which speed parameters are known. Most importantly, it is easy to incorporate this method in silicon compilation or logic synthesis tools. The parallel multiplier produced by the proposed method outperforms other schemes used for comparison in our experiment. It uses the minimal number of cells in the partial product reduction tree. These findings are tested on design examples simulated in 1 /spl mu/ CMOS ASIC technology.

[2] K.A.C.Bickerstaff, M.Schutle, and E.E. Swartzlander Jr., "Reduced area multipliers," Intl.Conf. on Application-Specific Array Processors, pp.478-489, 1993

This literature describes about, a high-speed

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method for the parallel multiplication of two binary numbers is to reduce their partial products to two numbers whose sum is equal to the product. The resulting two numbers are then summed using a fast carry-propagate adder. The authors present a multiplier, the reduced area multiplier, with a novel reduction scheme which results in fewer components and less interconnect overhead than either Wallace or Dadda multipliers. This reduction scheme is especially useful for pipelined multipliers, because it minimizes the number of latches required in the reduction of the partial products. Equations are given for determining the number of components and a method is presented for estimating the interconnect overhead for Wallace, Dadda and reduced area multipliers0

SIMULATION RESULTS

Here are the simulation results of Decimal Multiplication of two inputs (i.e., 5*5 =25). Where asa[3:0] and b[3:0] are 4-bit hexadecimal inputs, and p[7:0] is product which is output. Considering w,s,c – w[15:0] is a 16-bit intermediate wire, s[11:0] is a 12-bit intermediate sum and c[11:0] is also a 12-bit intermediate carry.

In order to reduce the power and area, the conventional Full adder in reduction phase of array multiplier is replaced by a modified full adder . In MUX based full adder the full adder is implemented using 4:1 multiplexers as shown in fig. 3. By implementing MUX based full adder in reduction phase of Array multiplier power reduction has been achieved. It is evident that, one 4:1 MUX can be made using three 2:1 MUX. The critical path delay can be written as shown below The array multiplier can be made more efficient by further reducing the critical path delay. The same can be achieved by using proposed full adder.

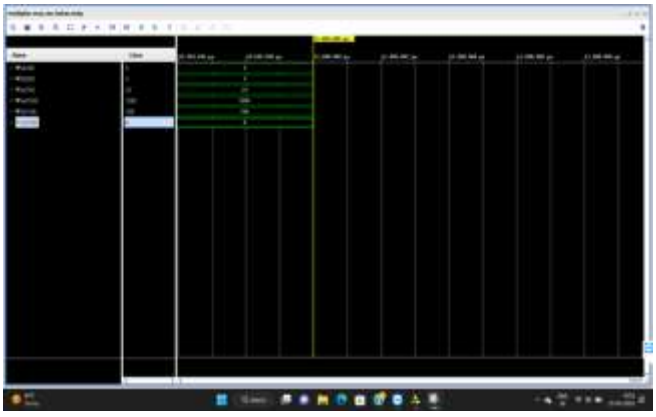

Fig.3: Simulation Output in decimal

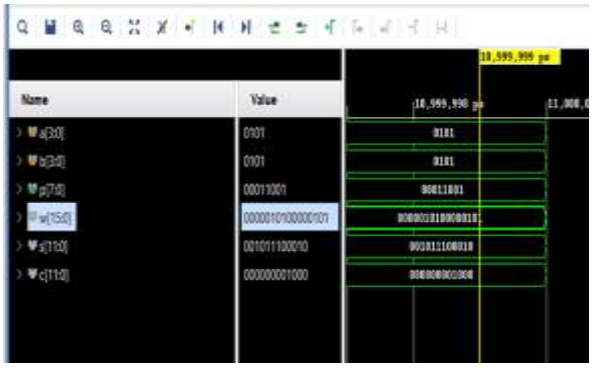

Fig.3: Simulation output in Binary

ADVANTAGES

- Less hardware
- Complexity is less
- Power Consumption is low
- Less Path Delays
- Mainly the multiplier focuses on the four aspects to form an efficient multiplier, i.e., speed, power consumption, area, and accuracy.

APPLICATIONS

- Digital signal processing
- Digital image processing
- Filters
- Arithmetic Logic Unit

- Processors
- Low power VLSI circuit Applications.

CONCLUSION

The proposed work describes low power, less complexity and less path delay by suitable design of Full Adder (i.e., Modified Full Adder) .The project is formulated based on the application of the Xilinx Vivado which is simulated and synthesized in Xilinx Vivado IDE using Verilog HDL.

VLSI technology is getting popularity in our society day by day. Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has been an important part in low- power VLSI system design . Fast multipliers are essential parts of digital signal processing systems. The speed of multiplier operation is of great importance in digital signal processing as well as in the general purpose processors today. The basic multiplication principle is twofold i.e., evaluation of partial products and accumulation of the shifted partial products. Mainly the multiplier focuses on the four aspects to form an efficient multiplier, i.e., speed, power consumption, area, and accuracy.

In this research, a low power-effective and simple Multiplier is designed. The optimization of adder has led to the improvement in performance of multiplier. In this paper, a modified full adder using multiplexer is modified to achieve low power consumption of multiplier. To analyze the efficiency of modified design, the conventional array multiplier structure is used. The designs are developed using Verilog HDL and the functionalities are verified through simulation using Xilinx. Hence, A low power and efficient multiplier is designed and implemented for various VLSI applications.

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