International Journal For Advanced Research In Science & Technology
A peer reviewed international journal
www.ijarst.in
ISSN: 2457-0362

# AN OPTIMIZED DESIG OF 64-BIT COMPARATOR BY USING REVERSIBLE LOGIC

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**ABSTRACT:** In this project, we present a comparator design using reversible gates. A need for low power ICs arises to keep the power density of ICs within tolerable limits. While the power dissipation increases linearly with advanced version processors, the power density also increases exponentially, because of the ever shrinking size of the integrated circuits. Reversible logic is emerging as an important research area in the recent years due to its ability to reduce power dissipation, which is the main requirement in low power digital design. In our proposed method reversible comparator based on CMOS logic circuit is designed using reversible gates. In this design we try to reduce optimization parameters like number of constant inputs, garbage outputs, and quantum cost. The experimental results obtained for implementation in Xilinx 80nm technology shows the considerable reduction in terms of area and Delay in comparison with the comparator designed using conventional gates. The design is simulated and verified using Xilinxtool.

**KEYWORDS:** Low power VLSI (Very large Scale Integrated) circuits, reversible gates, Comparator**.**

## I. INTRODUCTION

**Very-large-scale integration** (**VLSI**) is the process of creating an integrated circuit (IC) by combining hundreds of thousands of transistors or devices into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC designers add all of these into one chip.

Due to wide spread use of microprocessors and signal processors, implementation of high performance arithmetic hardware has always remained an attractive design problem. Arithmetic and Logic Unit (ALU) is the workhorse of microprocessors and determines the speed of operation of the processor. All modern processors include stand alone hardware for computation of basic arithmetic operations. In addition to fast arithmetic hardware, processors are also equipped with on-chip memory (cache) to achieve significant performance improvement by avoiding delay due to data access from main memory. The key objective of this work is to address the design of the functional blocks.

An Arithmetic Logical Unit is the very important subsystem in the digital system design. It is an integral part of a computer processor and a combinational logic unit that performs its arithmetic and logic operations. ALUs of various fixed bit-widths and full precision bit width are frequently required in very large-scale integrated circuits (VLSI) from processors to application specific integrated circuits (ASICs). Nowadays ALU is getting smaller and more complex to enable the development of a more powerful but smaller computer and processors. The need for high speed, less power consumption and compatible processors has been increasing as a result of computer, digital

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signal processing and networking applications. Arithmetic operations such as multiplication, addition, division and subtraction and logical operations such as AND, OR, NOT, XOR are using all type of processors used in various applications.

## II. EXISTED DESIGN

### Comparator Using Logic Gates

The conventional comparator uses standard gates neither like AND gate, OR gate, NOR gate, EX-NOR gate, NOT gate etc. The combinational blocks contains the AND Gate, OR Gate and NOR Gate. The block diagram of 4 bit comparator is given in the figure 1.The cascade logic is used to convert the 4bit comparator to 8 Bit and then 64 bit comparator. The block Diagram of 64 bit comparator is shown in figure (1).

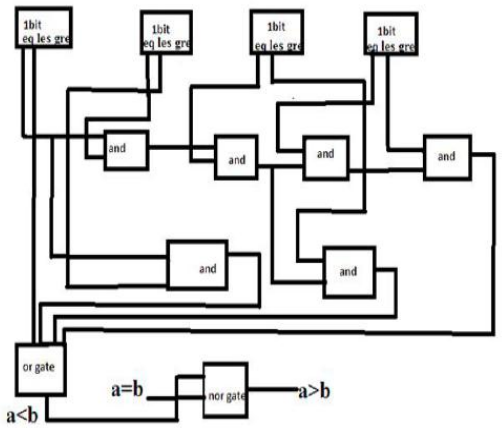


**Fig. 1: FUNCTIONAL DIAGRAM OF COMPARATOR ARCHITECTURE**

A low power 4 bit COMPARATOR is designed using Verilog HDL. Verilog HDL is an industry standard language for the description, modelling and synthesis or simulate of digital circuits and systems.

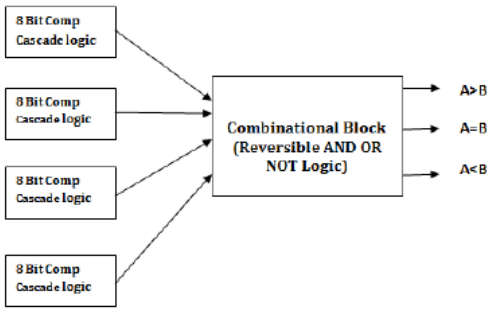


**Fig. 2: FUNCTIONAL BLOCK DIAGRAM OF 16-BIT COMPARATOR**

Addition is the most commonly used arithmetic operation and hence the performance of an ALU is greatly dependent on the performance of its adder. A variety of choices exists for addition depending on speed and area requirements.

**i. Equality Condition:** When all the AND gates produces the High Output then the condition is equal.

**ii. Less Than Condition:** If the equality condition fails the second level AND gate used checks for "less than" condition and finally the output of AND gate is given to OR gate along with equality condition to obtain the lesser condition

**iii. Greater Than Condition:** Simple NOR logic is used to find the greater than condition. The same logic is used for the implementation of 64 bit comparator also.

Chandni [3] The ALU is one of the most important module in a CPU and it can be modified during most instruction executions. So, more bit of operation of the ALU is important task. In this project 16 bit ALU is designed using VHDL and it is interfaced with RAM and ROM. This design is then implemented in Xilinx. After making an ALU interfaced it with RAM and ROM. All results are shown as waveforms in Xilinx software. This project helps to speed up the CPU. It can work fast and fewer instructions

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are required for the same operation compare to less bit ALU processor.

Nilam Patel [4], A design of general purpose processor with a 5 stage pipeline, to incorporate programmable resources in to a processor. RISC processors have a CPI (clock per instruction) of one cycle. This is due to the optimization of each instruction on the CPU and a technique called pipelining. This technique allows each instruction to be processed in a set number of stages. This in turn allows for the simultaneous execution of a number of different instructions, each instruction being at a different stage in pipeline. The development approach of the overall system design depends on the design specification, analysis and simulation. The RISC Processor core is high performance 32- bit microprocessor. This processor make it especially suited to embedded control applications.

DhanabalR [5] Arithmetic and Logic Unit (ALU) is one of the common and the most crucial components of an embedded system. Power consumption is a major design issue in the case of embedded systems. Usually ALU's consists of a number of functional units for different arithmetic and logic operations which are realized using combinational circuits. Each of the functional unit performs a specific arithmetic or logic operation. In this paper the main concern is given for reducing the power of the adder and multiplier modules which are important functional units of ALU thereby reducing the overall power consumption without compromising the speed of the processor. The ALU circuit ensures the execution of either arithmetic or logic operation only at a time so that only one set of circuits is active at a time thus ensuring low power consumption. The entire ALU circuit is realized using Verilog HDL and power analysis is obtained through same.

## III. PROPOSED SYSTEM

Reversible one bit comparator is implemented with Feynman gate and TR gate and BVF gate. The number of garbage outputs is one and represented as G1, it uses two constant inputs, logic 0 and logic 1 and its quantum cost is 7.If A=1, B=1 the F gate driving the output1 is 1 given to TR second input. The output2 of FG gate is 0 given to BVF gateinput2.These two gates output is fed to the input of BVF gate .Therefore the output of the AXOR is 1 which gives the equal condition. The block diagram of 1 Bit reversible comparator is shown in the figure 3.

### 3.1 FEYNMAN Gate

Feynman gate is also known as 2X2 reversible gate. The input and output vectors for Feynman gate is **In (A, B)** and **Out (P, Q)** respectively. The outputs of FEYMAN gate are denoted as P=A, Q=A XOR B and Quantum cost of a Feynman gate is one. The application of this gate is used in many circuits because of low cost of the FEYMAN gates.

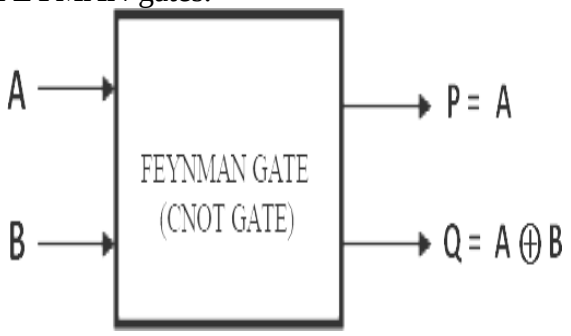


**Fig. 3: FEYNMAN GATE**

### 3.2 PERES Gate

It is also called as 3X3 reversible gate. The input and output vector for PERES gate is In

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(A, B, C) and Out (P, Q, R) respectively. The output is defined as P = A, Q = A XOR B and R=AB XOR C and the Quantum cost of Peres gate is 4. Because of its lowest quantum cost in many designs Peres gate is used. Half adder is designed by Single Peres gate.

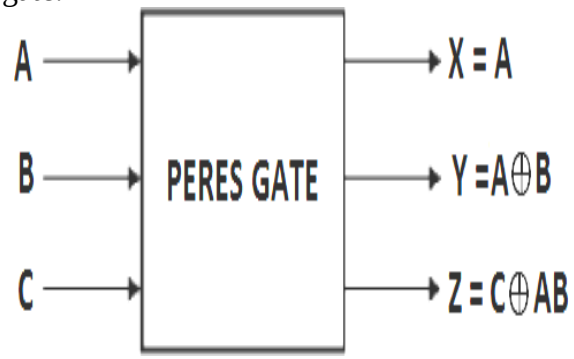


**Fig. 4: PERES GATE**

### 3.3 TOFFOLI Gate

Let IPv and OPv be the input and output vector of a 3*3 Toffoli Gate (TG) respectively, where IPv =(A, B, C) and OPv=(P=A, Q=B, R=AB⊕C). Fig 3 shows the 3*3 Toffoli gate. (Quantum Cost = 5).

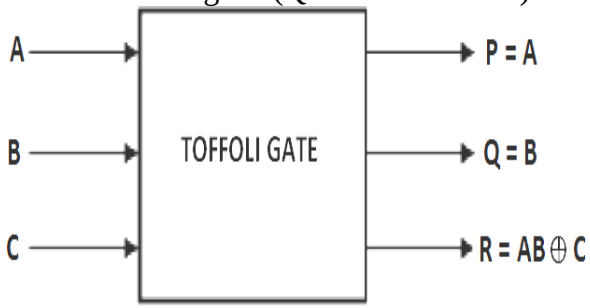


**Fig. 5: TOFFOLI GATE**

### 3.4 FREDKIN Gate

Let us consider IPv and OPv be the input and output vector of a 3*3 Fredkin Gate respectively, where IPv=(A,B,C) and OPv=(X=A,Y=A'B XOR AC , Z=A'C XOR AB). Fig 4 shows the Functional block diagram of 3*3 Fredkin gate. (Quantum Cost = 5)

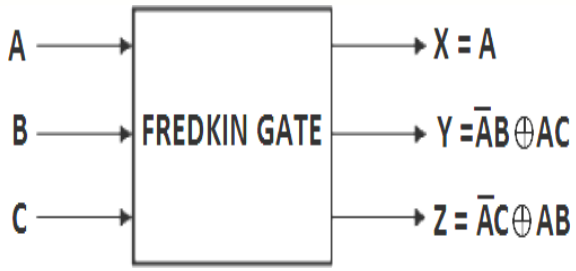


**Fig. 6: FREDKIN GATE**

### 3.5 BVF GATE:

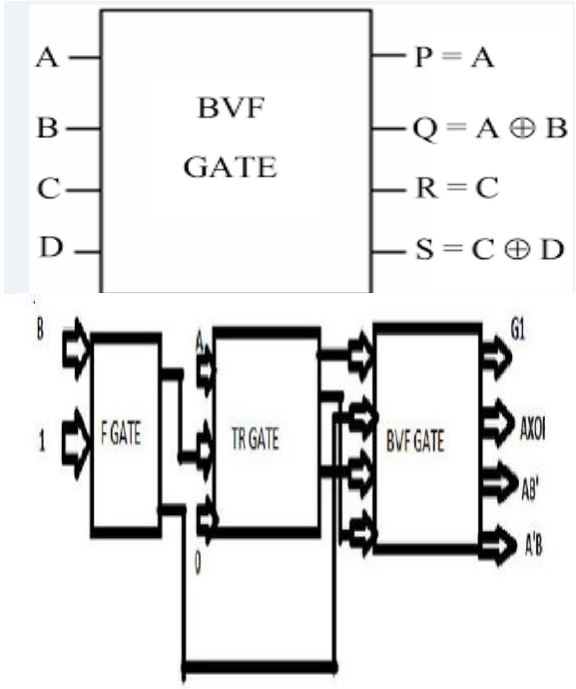


**Fig. 7: BVF GATE**

The reversible four bit comparator implemented using single bit comparator blocks designed using reversible gates. Reversible AND gate is designed by reversible Peres gate. Reversible OR and NOR gate is designed by Modified Toffoli gate. The cascading logic of 4 bit reversible comparator is used to construct the reversible 8 bit comparator. Similarly the 64 bit comparator is also constructed. The logic flow is same as the conventional 1-bit comparator. The reversible AND, OR, NOR. Gates are done Peres and Toffoli gate.

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## IV. RESULTS

The below figures shows the simulation output of implemented system as shown in the figure 8 where a, b are inputs and results is the output of the system.

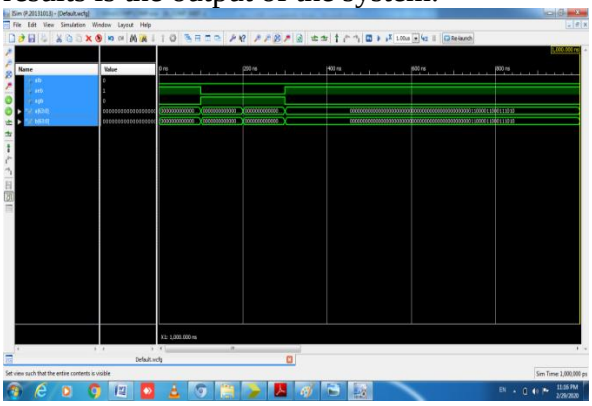

**Fig. 8: SIMULATION OUTPUT**

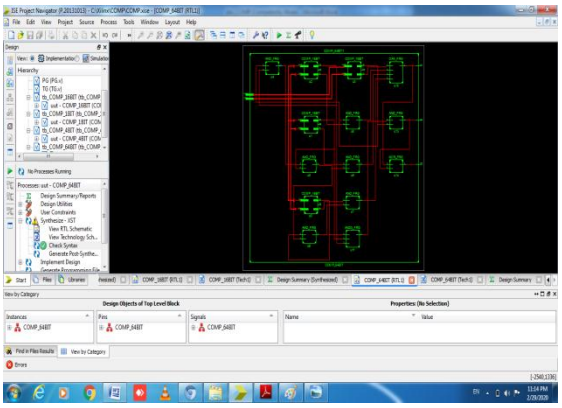

**Fig. 9: RTL SCHEMATIC OF IMPLEMENTED SYSTEM**

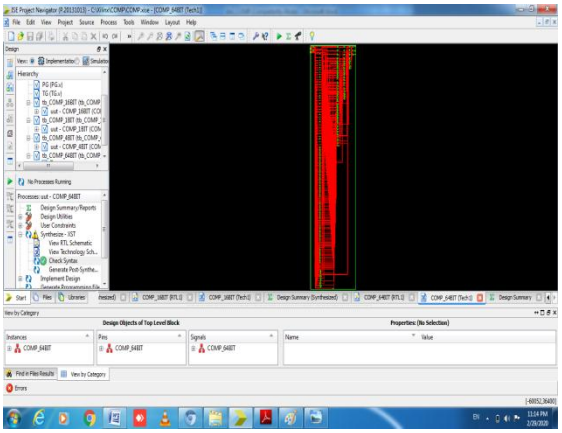

**Fig. 10: TECHNOLOGICAL SCHEMATIC**

**Table 1: COMPARISION TABLE**

| | Slices | LUT's | IOB's | Delay |
|---|---|---|---|---|
| **Existing** | **87** | **126** | **224** | **31.91ns** |
| **Implemented** | **44** | **74** | **171** | **12.09ns** |

From the above comparison table shows the comparison between existing and implemented design in terms of number of slices, LUT's, IOB's and delay. We can say that the implemented system is best in all factors compared to existing methods, thus the hardware is less for implemented design which means it has less area and power?

## V. CONCLUSION

The design has been able to achieve best power inflation over the past work in the same field. Also delay, power dissipation is compared between reversible and irreversible gates. The total area of FPGA which is used just 7 percentage of the complete area. Thus the design is upgraded to less amount of chip area. In this chapter, the RTL coding is done using Verilog, In order to synthesis this design the device named as "XC3S500E" has been chosen and the package as "FG320" with the device speed such as "-4". In synthesis process, the RTL model will be converted to the gate level net list mapped to a specific technology library. Here in this Spartan 3E family, many different devices were available in the Xilinx ISE tool. With this process we can get RTL, technology schematic and design summary, simulation results of the designs.

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