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PERFORMANCE ANALYSIS AND IMPLEMENTATION OF HIGH SPEED FULL-ADDER USING MODIFIED GDI TECHNIQUE

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ABSTRACT: A processor is a main part of any digital system. And an ALU is one of the main components of a microprocessor. To give a simple analogy, CPU works as a brain to any system & and ALU works as a brain to CPU. So it's a brain of computer's brain. They are consists of fast dynamic logic circuits and have carefully optimized structures. Rapid development of portable digital applications, the demand for increasing speed, compact implementation, and low power dissipation triggers numerous research efforts. The wish to improve the performance of logic circuits, once based on traditional CMOS technology, resulted in the development of many logic design techniques during the last two decades. GDI (Gate diffusion input) a technique of low power digital combinational design. This technique as compare to other currently used logic design styles, allows less power consumption and reduced propagation delay for low -power design of combinatorial digital circuits with minimum number of transistors. In this project presented with 4-bit arithmetic logical unit design with the use of Gate Diffusion Input Technique. And the ALU consist of 2*1 and 4*1 and full adder implementations. system robustness.

I.INTRODUCTION

A adder is one of the significant building In our day by day life, we utilize a great deal of compact electronic gadgets; these gadgets fundamentally are low force rapid VLSI circuits works at the same time. One of these circuits is the Arithmetic rationale unit (ALU) which considered a fundamental part in numerous applications, for example, Microprocessor, advanced sign handling, picture preparing, and so forth. Expansion considered basic piece of the number juggling unit and practically all other number-crunching activities incorporates expansion thusly any improvement in the viper cell is reflected as a significant improvement in the ALU. In this paper a 4-Bit ALU is planned utilizing a low force snake cell acknowledged by the Full-Swing GDI procedure

A processor is a fundamental piece of any advanced framework. What's more, an ALU is one of the principle segments of a microchip. To give a straightforward relationship, CPU functions as a cerebrum to any framework and ALU fills in as a mind to CPU. So it's a mind of PC's cerebrum. They are comprises of quick powerful rationale circuits and have deliberately enhanced structures. Of complete force utilization in any processor, CPU accounts a noteworthy part of it. ALU likewise add to one of the most powerful thickness areas on the processor, as it is timed at the most noteworthy speed and is occupied for the most part constantly which brings about warm hotspots and sharp temperature inclinations inside the execution center. In this manner , this rouse us emphatically for an energyefficient ALU structures that fulfill

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the elite prerequisites, while decreasing pinnacle and normal force dissipation.[1,2] Basically ALU is a combinational circuit that performs number juggling and sensible procedure on a couple of n bit operands for example A [0:7] and B [0:7] for 8 bits

II. GATE DIFFUSION INPUT (GDI)

Gate Diffusion Input (GDI) method is based on the utilization of a simple cell as shown in Fig. 1 which can be used for low power digital circuits [3]. This technique is implemented in twin-well CMOS or Silicon on Insulator (SOI) technologies. In this process, the bulks of both NMOS and PMOS transistors are hardwired to their diffusions to reduce the bulk effect that is dependence of threshold voltage on source-to-bulk voltage [12]. The dependence of transistor threshold voltage on source-to-bulk voltage is as follows:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{\left|2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right) - \eta V_{DS}$$

Where VSB is source-body voltage, Vth0 is threshold voltage at VSB=0, γ is linearized body coefficient, ΦF is the Fermi potential and η is Drain nduced Barrier Lowering (DIBL) coefficient. Using this procedure power consumption can be reduced along with delay time thereby delivering a reduced power delay product. Consequently area of the circuit is minimized.

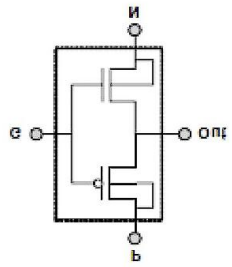

Figure 1: Basic GDI Cell

It should be noted that though the circuit resembles with standard CMOS inverter, there are certain important differences compared to conventional one. The GDI cell contains 3 inputs— P which is the input to the outer diffusion node of the PMOS transistor is not connected to Vdd while N which is the input to the outer diffusion node of the NMOS transistor is not connected to GND, and G which is the common gate input of both the NMOS and PMOS transistors. The Out node which is the common diffusion of both the transistors may be utilized as input or output port depending on the circuit configuration.

The ports P and N delivers 2 extra pins which yield the GDI design more compliant than the usual CMOS design [3]. Fig. 2 shows the transient response of a GDI cell which is quite similar to that of a standard CMOS inverter [13], [14]. This analysis is based on the Shockley model in which the drain current ID is represented as shown below

$$I_D = \begin{cases} I_{D0}\left(\frac{W}{L}\right) e^{(qV_{GS}/KT)} \\ \quad (V_{GS} \le V_{TH} : \text{subthreshold region}) \\ K\left\{(V_{GS} - V_{TH})V_{DS} - 0.5V_{DS}^2\right\} \\ \quad (V_{DS} < V_{GS} - V_{TH} : \text{linear region}) \\ 0.5K(V_{GS} - V_{TH})^2 \\ \quad (V_{DS} \ge V_{GS} - V_{TH} : \text{saturation region}) \end{cases}$$

Where K denotes device trans conductance parameter, VTH denotes threshold voltage, W denotes channel width and L denotes channel length.

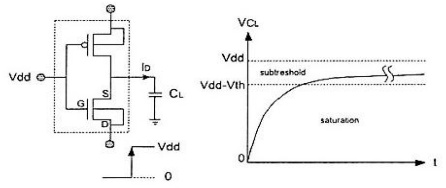

Figure 2: Transient response of a GDI cell

However, it is to be mentioned that in GDI cell Vds has to be considered as a variable

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of input voltage in Shockley model [3] in contrast with CMOS inverter analysis [15] where Vgs was considered as an input voltage.

III.LOGIC GATES BASED ON GDI METHOD

Table I shows the various operations that can be performed with a basic GDI cell.

TABLE I. DIFFERENT OPERATIONS OF BASIC GDI CELL

N	P	G	Out	Operation
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}$+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B$+AC	MUX
'0'	'1'	A	$\bar{A}$	NOT

From table I, it can be noticed that using only 2 transistors various functions can be performed. For instance, OR gate can be designed using a single GDI cell whereas in case of designing of an OR gate gate can be designed using only 2 transistors and even a Multiplexer MUX) can be devised using a single GDI cell. Thus, a simple alteration to the input configuration of the GDI cell would yield myriad variety of Boolean functions. Multiple-input gates can be implemented by combining several GDI cells.

IV PROPOSED SYSTEM

Full adder is a combinational circuit that Gate Diffusion Input Technique is another strategy for lessening power dissemination, spread postponement with less territory. We have structured ALU in various manner by utilizing GDI cells to actualize multiplexers and full viper circuit. The info and yield areas comprise of 4x1 and 2x1 multiplexers and ALU is actualized by utilizing full adder.Ex: T. Esther Rani, M. Asha Rani, Dr. Rameshwar Rao, planned a zone advanced low force number juggling and rationale unit in which Arithmetic Logic Unit is actualized utilizing rationale doors, pass transistor rationale, just as GDI procedure

A multiplexer is a computerized switch picks the yield from a few sources of info dependent on a select sign [4], appeared in Fig. 2 a 2x1 multiplexer comprises of 6 transistors.

A number juggling rationale unit (ALU) is a crucial structure square of the Central Processing Unit (CPU) of a PC, and even the most straightforward microchips contain one. It is liable for performing number juggling and rationale tasks, for example, expansion, deduction, increase, decrement, sensible AND, legitimate OR, intelligent XOR and consistent XNOR.ALU comprises of eight 4x1 multiplexers, four 2x1 multiplexers and four full adders. The 4-piece ALU is structured in 250nm, n-well CMOS innovation. At the point when rationale '1'and rationale '0' are applied as an info INCREMENT and DECREMENT tasks happens separately. An INCREMENT activity is dissected as including '1' to the numbers to be added and DECREMENT is viewed as a deduction activity [6].

TABLE II. TRUTH TABLE OF THE PROPOSED 4-BIT ALU.

S2	S1	S0	Operations
0	0	0	DECREMENT
0	0	1	ADDITION
0	1	0	SUBSTRACTION
0	1	1	INCREMENT
1	0	0	AND
1	0	1	XOR
1	1	0	XNOR
1	1	1	OR

Two's complement method is used for SUBTRACTION in which complement of B is used. The outputs obtained from the full

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adder are SUM, EXOR, EXNOR, AND & OR.

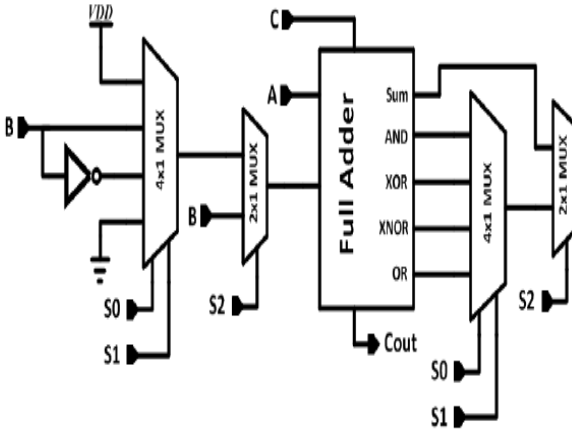

Fig:4.2 shows the square chart of 4-piece ALU where the primary stage to fourth stage is fell with the CARRY bit. Emblematic portrayal of 4-piece ALU has been envisioned in fig. 3. The multiplexer stage chooses the suitable sources of info dependent on the state of the select signals, and offers it to the full snake which at that point processes the outcomes. The multiplexer at the yield stage chooses the suitable yield and course it to yield port. The activity being performed and the data sources and yields being chosen are controlled by set of three select signs consolidated in the structure. Fig 8. shows multiplexer rationale at input port and Fig 9. shows multiplexer rationale at yield port. The multiplexer stage chooses the proper data sources dependent on the state of the select signals, and offers it to the full viper which at that point figures the outcomes. The multiplexer at the yield stage chooses the suitable yield and course it to yield port. Table 2 shows reality table for the tasks performed by the ALU dependent on the status of the select sign.

V IMPLEMENTATION

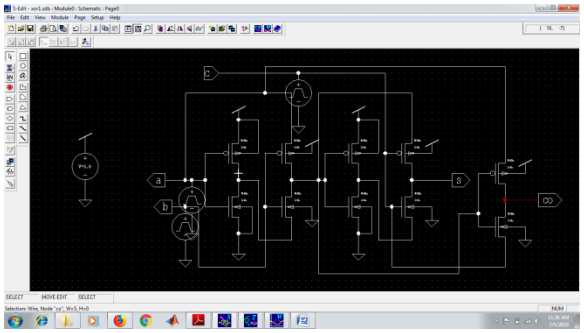

Fig 5 Circuit Design

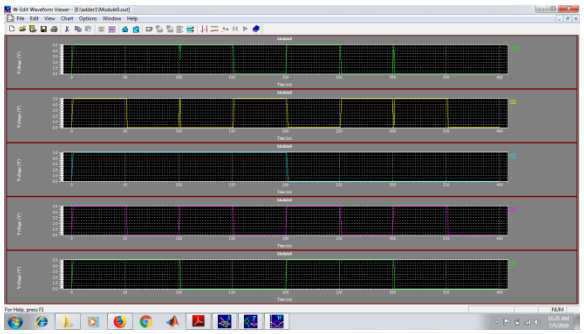

Fig 5 Simulation Result

VI CONCLUSION

The goal of this paper was to design a full adder with high speed performance using GDI technique. From the performance analysis table it is clear that the proposed design system is the best among the discussed designs in terms of area, delay and power dissipation. Since the results were obtained as an outcome of simulation, the readings are precise. This design will have an improved speed and also the efficiency of the system is more compared to all the conventional techniques. Further modifications can be made in the design by adding a few more transistors.

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